AMD

AMD PowerNow!™ Technology Platform Design Guide for Embedded Processors

Application Note

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Revision History

Date	Rev	Description
December 2000	A	Initial public release.

Application Note

AMD PowerNow!™ Technology Platform Design Guide for Embedded Processors

AMD PowerNow!™ Technology Initiative

AMD's latest power-saving initiative, AMD PowerNow!™ technology, enables embedded system designers to offer superior performance.

AMD PowerNow! technology uses combinations of CPU core voltage and frequency (AMD PowerNow! technology states) to enable maximum performance in any thermal environment, while providing the embedded system designer with the ability to finely tune performance dependent upon the specific demands of the application.

Table 1 on page 2 shows the basic set of AMD PowerNow! technology operational modes or states. However, AMD PowerNow! technology is not restricted to the operation modes listed.

Additionally, AMD PowerNow! technology can be used in conjunction with existing power management schemes, such as Advanced Configuration and Power Interface (ACPI). This allows AMD PowerNow! technology to optimize the performance and power savings of a device.

Table 1. Basic Set of AMD PowerNow!™ Technology Operational Modes

Operational Mode	Description	Application Power
High-Performance	Operation at peak frequency and voltage, maximizing performance within thermal constraints	< 12 W
Automatic	Core voltage and frequency are scaled to exactly meet application demand and conserve power usage	3–11 W
Power-Saver	Operation at lowest supported frequency and voltage to maximize power efficiency	< 3 W

Overview of this Document

This document identifies and describes the key components of AMD PowerNow! technology as they apply to embedded system designers desiring to incorporate AMD PowerNow! technology features. Unless otherwise noted, the terms CPU or processor refer to the AMD-K6™-2E+ and/or the AMD-K6™-IIIE+ processor built in 0.18-micron process technology.

Specifically, this document addresses the following:

- Identification of the Enhanced Power Management (EPM) features designed in the 0.18-micron AMD-K6-2E+ and the AMD-K6-IIIE+ processors for supporting AMD PowerNow! technology.
- Description of how the EPM features can be incorporated to create embedded platforms enabled with AMD PowerNow! technology.
- Description of design considerations including new processor pinouts, voltage regulator recommendations, and other implementation options specific to designing with AMD PowerNow! technology.

Note: *The information presented in this document is preliminary and subject to change.*

Enhanced Power Management Features

AMD-K6-2E+ and AMD-K6-IIIE+ low-power processors enabled with AMD PowerNow! technology include two new features specifically designed to enhance power management functionality:

- Dynamic core frequency control
- Core voltage control

These enhanced power management (EPM) features are accessed and controlled through an aligned 16-byte block of I/O address space that is defined by a model-specific register (MSR) called the Enhanced Power Management Register (EPMR).

Enhanced Power Management Register (EPMR)

The EPMR register allows software to access the aligned EPM 16-byte block of I/O address space, which contains bits for enabling, controlling, and monitoring the EPM features. All accesses to the EPM 16-byte I/O block must be aligned dword accesses. Valid accesses to the EPM 16-byte block do not generate I/O cycles on the host bus, keeping EPMR accesses local to the CPU, while non-aligned and non-dword accesses are passed to the host bus.

Figure 1 on page 4 and Table 2 define the EPMR register. The EPMR can be addressed at MSR location C000_0086h.

An assertion of RESET clears all of the bits of the 16-byte I/O block to 0 (excluding the Voltage ID Output bits which default to 01010b). BIOS or the real-time operating system (RTOS) must always initialize the EPMR register and EPM features after the processor comes out of RESET.

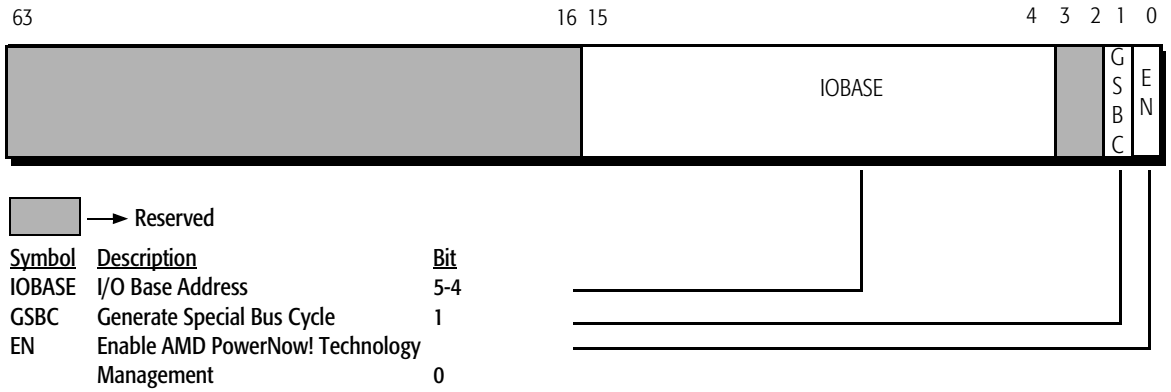

Figure 1. Enhanced Power Management Register (EPMR)

Table 2. Enhanced Power Management Register (EPMR) Definition

Bit	Description	R/W	Function[1]
63–16	Reserved	R	All reserved bits are always read as 0.
15-4	I/O BASE Address (IOBASE)	R/W	IOBASE defines a base address for a 16-byte block of I/O address space accessible for enabling, controlling, and monitoring the EPM features.
3-2	Reserved	R	All reserved bits are always read as 0.
1	Generate Special Bus Cycle (GSBC)	R/W	This bit controls whether a special bus cycle is generated upon dword accesses within the EPM 16-byte I/O block. If set to 1, an EPM special bus cycle is generated, where BE[7:0]# = BFh and A[4:3] = 00b.
0	Enable AMD PowerNow! Technology Management (EN)	R/W	This bit controls access to the I/O-mapped address space for the AMD PowerNow! technology EPM features. Clearing this bit to zero does not affect the state of bits defined in the EPM 16-byte I/O block.

Notes:
1. All bits default to 0 when RESET is asserted.

IOBASE Field

The EPM 16-byte I/O block is located at the I/O address specified by the IOBASE field and is initialized during power-on self test (POST) by the BIOS or RTOS. The EPM 16-byte I/O block is then used to access the EPM features.

The EPM features are hidden from all application software and need only be accessible by an RTOS or an SMM handler for Microsoft® operating systems. Therefore, the BIOS does not need to report the I/O range to the operating system.

GSBC Bit

If the GSBC bit is enabled (set to 1), a special bus cycle is generated once a dword access is made within the EPM 16-byte I/O block. The EPM special bus cycle is defined by the processor driving D/C# low, M/IO# low, W/R# high, BE[7:0]# to BFh and A[31:3] to 0000h. The system logic must return BRDY# in response to all processor special cycles.

EN Bit

The Enable AMD PowerNow! Technology Management (EN) bit should only be enabled (set to 1) by the RTOS, BIOS, or SMM handler when attempting to access the EPM features.

Upon exiting, the EN bit should be disabled to protect the EPM 16-byte I/O block from spurious activity. When the EN bit is disabled, accesses to the EPM block 16-byte I/O block are passed to the host bus.

EPM 16-Byte I/O Block

The EPM 16-byte I/O block contains a single 4-byte field for enabling, controlling, and monitoring the EPM features. This Bus Divisor and Voltage ID Control (BVC) field (see Figure 2, "Dynamic Core Frequency Control" on page 10, and Figure 3 on page 11) is the control center for supported state transitions. Table 3 defines the functions supported by each of the byte-fields within the EPM 16-byte I/O block.

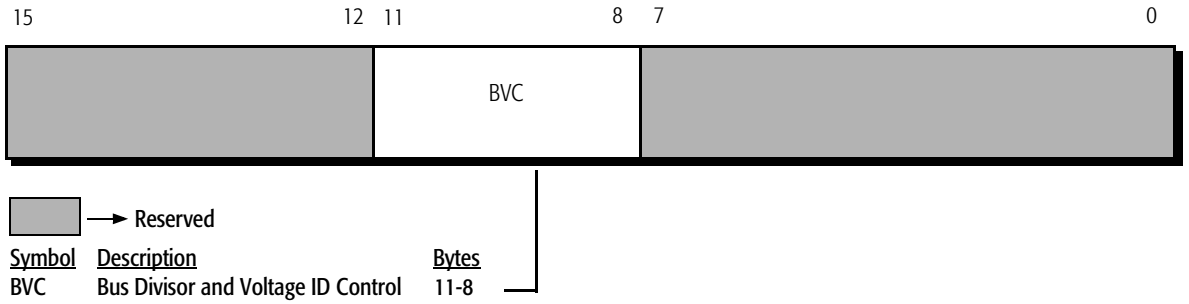

Figure 2. EPM 16-Byte I/O Block

Table 3. EPM 16-Byte I/O Block Definition

Byte	Description	R/W	Function[1]
15-12	Reserved	R	All reserved bits are always read as 0.
11-8	Bus Divisor and Voltage ID Control (BVC)	R/W	The bit fields within the BVC bytes allow software to change the processor bus divisor and core voltage. See "Dynamic Core Frequency Control" on page 10 and Figure 3 on page 11 for detailed information about this field.
7-0	Reserved	R	All reserved bits are always read as 0.

Notes:
1. All bits default to 0 when RESET is asserted

Dynamic Core Frequency and Core Voltage Control

AMD-K6-2E+ and AMD-K6-IIIE+ processors enabled with AMD PowerNow! technology support the ability to change the bus frequency divisor and core voltage seamlessly during run time. These features are implemented in conjunction with a new clock control state—the EPM Stop Grant state.

To invoke an AMD PowerNow! technology state transition, the desired settings for core voltage and processor frequency are written to the Voltage ID Output (VIDO) and Internal BF Divisor (IBF) fields of the BVC field. The EPM Stop Grant state and state transition then occur automatically by writing a 1 to the Generate Special Bus Cycle (GSBC) bit in the EPMR and a non-zero value to the Stop Grant Time-out Counter (SGTC) field.

For Microsoft operating systems, the EPMR register should be accessed using an SMM handler. In these environments, the SMM handler can initiate a special bus cycle for core voltage and frequency transitions by writing a 1 to the GSBC field in the EPMR and a non-zero value to the SGTC.

- This action enables the processor to enter the EPM Stop Grant State and transitions the CPU core voltage and frequency to the values specified in the VIDO and IIBF fields of the BVC field.
- Once the SGTC period has expired, the EPM Stop Grant state is exited and the AMD PowerNow! technology state transition is completed.

Effective Bus Divisors EBF[2:0]

The processor core frequency is controlled by the Effective Bus Frequency Divisor—EBF[2:0]—which dictates the processor-to-bus clock ratio supplied to the processor's internal PLL. This processor-to-bus clock ratio is multiplied by the external bus frequency to set the frequency of operation for the processor core.

- At the fall of RESET, the EBF[2:0] value is determined by the state of the processor BF[2:0] input pins.
- Afterwards, the EBF[2:0] value can be dynamically controlled through AMD PowerNow! technology state transitions.

Table 4 lists valid EBF[2:0] states and equivalent processor- to-bus clock ratios.

Table 4. Processor-to-Bus Clock Ratios

State of EBF[2:0]	Processor-to-Bus Clock Ratio
100b	2.0x[1]
101b	3.0x
110b	6.0x
111b	3.5x
000b	4.5x
001b	5.0x
010b	4.0x
011b	5.5x

Notes:

1. The 0.18-micron processors do not support the 2.5x ratio supported by earlier processors. Instead, a ratio of 2.0x is selected when EBF[2:0] equals 100b

BF[2:0] Strapping Considerations

Systems that do not use the AMD PowerNow! technology dynamic core frequency control mechanism should strap the BF[2:0] inputs of the CPU (with pull-up/pull-down resistors) to select the desired CPU operating frequency at power up.

Systems that use AMD PowerNow! technology dynamic core frequency control mechanisms have two primary strapping options for the BF[2:0] inputs:

- Strap the BF[2:0] inputs to select the maximum CPU core frequency at power up *(recommended)*
- Strap the BF[2:0] inputs to select the minimum CPU core frequency at power up

Selecting Maximum CPU Core Frequency

Systems can strap the BF[2:0] inputs to allow the processor to boot at its maximum rated frequency when RESET is asserted. BIOS can then determine the maximum frequency of the processor by reading the PSOR model-specific register, which stores the state of the EBF[2:0] bits. For more information on the PSOR register, see the *Embedded AMD-K6™ Processors BIOS Design Guide Application Note*, order# 23913.

See "Safe Voltage and Frequency Combination at Reset" on page 20 for the advantages and disadvantages of booting at maximum core frequency.

Selecting Minimum CPU Core Frequency

Systems that strap the processor BF[2:0] inputs to 100b allow the processor to boot with a core frequency of 2.0x the processor bus frequency when RESET is asserted. If a different CPU core frequency is desired prior to loading the OS, it is the responsibility of the BIOS, early in the POST routine, to transition the processor core frequency and voltage to the desired performance level.

See "Safe Voltage and Frequency Combination at Reset" on page 20 for the advantages and disadvantages of booting at a minimum core frequency.

Dynamic Core Frequency Control

For Microsoft operating systems, the BVC field of the EPM 16-byte I/O block is accessed through an SMM handler.

- To invoke a new processor core frequency, the SMM handler initiates core voltage and frequency transitions by writing a 1 to the GSBC field in the EPMR and a non-zero value to the SGTC.
- This action initiates a special bus cycle to place the processor into the EPM Stop Grant state and transitions the CPU core voltage and frequency to the values specified in the VIDO and IBF fields of the BVC field.

Note: *System-initiated inquire (snoop) cycles are not supported and must be prevented by the BIOS or operating system while in the EPM Stop Grant state.*

BVC Field

Figure 3 on page 11 shows the format and Table 5 defines the function of each bit of the BVC field located within the EPM 16-byte I/O block.

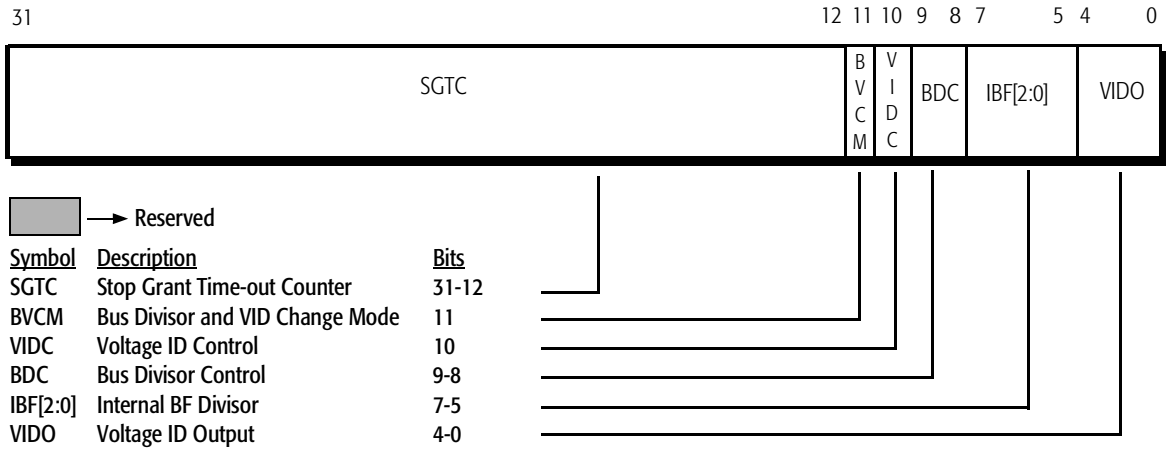

Figure 3. Bus Divisor and Voltage ID Control (BVC) Field

Table 5. Bus Divisor and Voltage ID Control (BVC) Definition

Bit	Description	R/W	Function[1]
31-12	Stop Grant Time-out Counter (SGTC)	W	Writing a non-zero value to this field causes the processor to enter the EPM Stop Grant state internally. This 20-bit value is multiplied by 4096 to determine the duration of the EPM Stop Grant state, measured in processor bus clocks.
11	Bus Divisor and VID Change Mode (BVCM)	R/W	This bit controls the mode in which the bus-divisor and the voltage control bits are allowed to change. If BVCM=0, the Bus Divisor and Voltage ID changes take effect only upon entering the EPM Stop Grant state as a result of the SGTC field being programmed. BVCM=1 is reserved.
10	Voltage ID Control (VIDC)	R/W	This bit controls the mode of Voltage ID control. If VIDC=0, the processor VID[4:0] pins are unchanged upon entering the EPM Stop Grant state. If VIDC=1, the processor VID[4:0] pins are programmed to the VIDO value upon entering the EPM Stop Grant state. *BIOS should initialize this bit to 1 during the POST routine.*
9-8	Bus Divisor Control (BDC)	R/W	This 2-bit field controls the mode of Bus Divisor control. If BDC[1:0]=00b, the BF[2:0] pins are sampled at the falling edge of RESET. If BDC[1:0]=1xb, the IBF[2:0] field is sampled upon entering the EPM Stop Grant state. BDC[1:0]=01b is reserved. *BIOS should initialize these bits to 10b during the POST routine.*
7-5	Internal BF Divisor (IBF)	R/W	If BDC[1:0]=1xb, the processor EBF[2:0] field of the PSOR is programmed to the IBF[2:0] value upon entering the EPM Stop Grant state.
4-0	Voltage ID Output (VIDO)	R/W	This 5-bit value is driven out on the processor VID[4:0] pins upon entering the EPM Stop Grant state if the VIDC bit=1. These bits are initialized to 01010b and driven on the processor VID[4:0] pins at RESET.

Notes:

1. All bits default to 0 when RESET is asserted, except the VIDO bits which default to 01010b

Voltage Identification (VID) Outputs

AMD-K6-2E+ and AMD-K6-IIIE+ low-power processors enabled with AMD PowerNow! technology feature Voltage ID (VID) outputs to support dynamic control of the core voltage. These outputs should serve as inputs to a DC/DC regulator that supplies the processor core voltage. Based on its VID[4:0] inputs, the regulator outputs a corresponding voltage. (See "Hardware Implementation" on page 18 for more detailed information on using the VID outputs in embedded systems.)

For regulators that do not support VID inputs, the processor's VID[4:0] outputs must be used to manipulate the regulator's feedback voltage to vary the regulator output voltage.

It is not necessary to drive all of the processor VID[4:0] outputs to the voltage select inputs of the DC/DC regulator. Any voltage select inputs of the DC/DC regulator that are not driven by the processor VID[4:0] outputs should be tied to ground.

All VID[4:0] Output Pins Used

System implementations that incorporate all processor VID outputs typically support a voltage range of 0.925 V to 2.0 V. Table 6 on page 13 lists VID[4:0] codes that are typical for DC/DC regulators.

Subset of VID[4:0] Outputs Used

System implementations that use a subset of the processor VID outputs will require external logic to translate the processor VID pins into a full five-bit DC/DC regulator input code.

One solution that is recommended for a maximum BF[2:0] boot strap option (see page 9) requires that regulator D[4] and D[0] inputs be connected to GND while inputs D[3:1] are connected to the processor VID[4], VID[2], and VID[0] outputs, respectively, through external logic.

For a 2.1-V core voltage implementation, the available core voltage is thereby limited to a range of 1.36 V to 2.1 V in approximately 100-mV increments, but the rework and external logic cost is minimal. Table 7 on page 13 shows the voltage translation using the Max1711 DC/DC regulator.

Unused VID[4:0] Outputs

System designs that do not use the dynamic core voltage control feature provided in AMD PowerNow! technology should simply leave the processor VID[4:0] outputs as no-connects (NC) on the motherboard.

Table 6. VID [4:0] Input-to-Output Voltage Codes (Typical for DC/DC Regulators)

VID Inputs					Output Voltage
D[4]	D[3]	D[2]	D[1]	D[0]	
0	0	0	0	0	2.00 V
0	0	0	0	1	1.95 V
0	0	0	1	0	1.90 V
0	0	0	1	1	1.85 V
0	0	1	0	0	1.80 V
0	0	1	0	1	1.75 V
0	0	1	1	0	1.70 V
0	0	1	1	1	1.65 V
0	1	0	0	0	1.60 V
0	1	0	0	1	1.55 V
0	1	0	1	0	1.50 V
0	1	0	1	1	1.45 V
0	1	1	0	0	1.40 V
0	1	1	0	1	1.35 V
0	1	1	1	0	1.30 V
0	1	1	1	1	Shutdown[1]

VID Inputs					Output Voltage
D[4]	D[3]	D[2]	D[1]	D[0]	
1	0	0	0	0	1.275 V
1	0	0	0	1	1.250 V
1	0	0	1	0	1.225 V
1	0	0	1	1	1.200 V
1	0	1	0	0	1.175 V
1	0	1	0	1	1.150 V
1	0	1	1	0	1.125 V
1	0	1	1	1	1.100 V
1	1	0	0	0	1.075 V
1	1	0	0	1	1.050 V
1	1	0	1	0	1.025 V
1	1	0	1	1	1.000 V
1	1	1	0	0	0.975 V
1	1	1	0	1	0.950 V
1	1	1	1	0	0.925 V
1	1	1	1	1	Shutdown[1]

Notes:

1. *If the voltage regulator is to be powered when the processor is to be powered off (for example, during Suspend to RAM), it is necessary to assert the regulator's shutdown pin to power off the processor.*

Table 7. Regulator Solution Using a Subset of CPU VID Outputs

Max1711 Regulator D[4:0] Inputs	Connection to CPU VID Outputs	CPU VID[4:0] Outputs[1]	Regulator D[4:0] Inputs[2]	Voltage Selected[3]
D[4]	GND	0x0x0	00000	2.00 V
D[3]	CPU VID[4][4]	0x0x1	00010	1.90 V
D[2]	CPU VID[2][4]	0x1x0	00100	1.80 V
D[1]	CPU VID[0][4]	0x1x1	00110	1.70 V
D[0]	GND	1x0x0	01000	1.60 V
		1x0x1	01010	1.50 V
		1x1x0	01100	1.40 V
		1x1x1	01110	1.30 V

Notes:

1. *CPU VID[3] and VID[1] are each treated as an NC (no-connect) and represented by "x".*
2. *Regulator D[4] and D[0] are tied to GND.*
3. *Assumes a resistor divide circuit is used with the regulator to support a 2.1-V core voltage.*
4. *CPU VID[4], VID[2], and VID[0] are connected to the regulator through external logic.*

Guaranteed CPU Core Voltage at Power On

The processor VID[4:0] outputs are initialized to a default state of 01010b, but they are only initialized after RESET is asserted, the CPU input clock is running, and an I/O voltage is applied. As a result, it is necessary to drive the input select pins of the DC/DC regulator from a source other than the CPU during system power up.

This can be accomplished by placing external logic between the VID[4:0] outputs of the processor and the voltage select inputs of the DC/DC regulator. The System Power Good (SPWRGD) signal can then be used as an input to the external logic to strap the DC/DC regulator's voltage select inputs to the desired state until the processor's VID[4:0] outputs have been initialized.

- When SPWRGD is negated, the external logic drives the selected strap value to the regulator's D[4:0] inputs.
- When SPWRGD is asserted, the external logic allows the CPU VID[4:0] outputs to drive the regulator's D[4:0] inputs.

Note: *The SPWRGD signal must only assert after all power good signals (I/O, core, +5-V, etc.) are asserted.*

For a minimum BF[2:0] boot strap option (see page 9), a multiplexer and the SPWRGD signal can be used for this purpose.

For a maximum BF[2:0] boot strap option (see page 9), a multiplexer function is incorporated through the recommended AND-gate solution discussed in "Subset of VID[4:0] Outputs Used" on page 12.

In both cases, the SPWRGD signal, when equal to 0, forces the VID[4:0] outputs of the external logic to a value equivalent to the output state that the processor drives on its VID[4:0] pins when SPWRGD transitions to a 1. Once RESET is negated, BIOS is free to transition the processor core frequency and voltage as needed.

Figure 5 on page 25 helps to illustrate the concept of implementing a guaranteed CPU core voltage at power on.

Dynamic Core Voltage Control

For Microsoft operating systems, the BVC field of the EPM 16-byte I/O block is accessed through an SMM handler. To invoke a new processor core voltage, the SMM handler initiates core voltage and frequency transitions by writing a 1 to the GSBC field in the EPMR and a non-zero value to the SGTC. This action automatically places the processor into the EPM Stop Grant state and transitions the CPU core voltage to the value specified in the VIDO field of the BVC field.

Note: *System-initiated inquire (snoop) cycles are not supported and must be prevented by the BIOS or operating system while in the EPM Stop Grant state. This is typically accomplished through the use of the ACPI-defined ARB_DIS control bit, which turns off the PCI bus arbiter in the north bridge.*

The VID[4:0] outputs are determined by the value stored in the VIDO field within the BVC field of the 16-byte I/O block during AMD PowerNow! technology state transitions. For more information on the format and definition of the BVC field, see “BVC Field” on page 10.

AMD PowerNow! Technology Initialization

Initialization of the AMD-K6-2E+ and AMD-K6-IIIE+ low-power processors is straightforward. Below is a complete summary illustrating the actions required to properly initialize these processors for implementation of AMD PowerNow! technology.

Software Initialization

Detailed information for effective software control of devices enabled with AMD PowerNow! technology is provided in the "Software Implementation" section, beginning on page 28.

To initialize the software:

- Write the I/O base address (IOBASE) field (EPMR[15:4]) for the 16-byte EPM I/O block. This sets up the location in the I/O map where the EPM I/O block will reside. Be sure to locate the EPM I/O block so that it does not conflict with other system I/O-mapped resources. The EPMR is accessed at MSR location C000_0086h.
- Clear the Enable AMD PowerNow! Technology Management (EN) bit (EPMR[0]) to disable address decodes of the EPM I/O block fields. Clearing EPMR[0] ensures that errant writes to I/O space do not accidentally change the AMD PowerNow! technology state. For Windows desktop-based operating systems, the SMI handler will set EPMR[0]=1b only when SMM is entered for the purpose of doing an AMD PowerNow! technology state transition. Real-time operating systems should set EPMR[0]=1b only when attempting an AMD PowerNow! technology state transition. This bit may be cleared in the same MSR write that initializes the EPM I/O block base.

Note: *EPMR[0] should be cleared upon completing any AMD PowerNow! technology state transition to ensure errant writes to I/O space do not inadvertently alter the AMD PowerNow! technology state of the processor.*

- The VIDC bit (BVC[10]) should be set to 1 at power-on self test (POST). **All subsequent writes to this field should ensure that this bit equals 1b at all times.** Initializing this bit causes a read/modify-bit/write operation on the BVC field. After reading the BVC field and setting the VIDC bit during initialization, be sure to clear all bits in the SGTC field before writing the BVC field back out. This is required because the data returned in the SGTC field is invalid, as it is a write-only field.

Note: *Both the VIDC and BDC bits may be initialized at the same time.*

- The BDC field (BVC [9:8]) should be set to 10b at POST. **All subsequent writes to this field should ensure that these bits remain 10b at all times.** After reading the BVC field and setting the BDC bits during initialization, be sure to clear all bits in the SGTC field before writing the BVC field back out. This is required because the data returned in the SGTC field is invalid, as it is a write-only field.

Note: *Both the VIDC and BDC bits may be initialized at the same time.*

- Make the AMD PowerNow!™ Technology Descriptor Table (see page 30) visible in the system memory map on a 16-byte boundary within the range of 0x0C0000–0x0FFFFF or within the first Kbyte of the extended BIOS data area.

Hardware Initialization

Information on implementing an efficient AMD PowerNow! technology device is provided in the "Hardware Implementation" section, beginning on page 18.

To initialize the hardware:

- Strap the system for one of the recommended power-up configurations: maximum CPU frequency or minimum CPU frequency setting. See "Safe Voltage and Frequency Combination at Reset" on page 20 for details.
- At reset, both the AMD-K6-2E+ and AMD-K6-IIIE+ low-power processors drive 01010b on the VID[4:0] pins. The VID-capable voltage regulator and implementation must be equipped to handle this signaling at reset. See "Safe Voltage and Frequency Combination at Reset" on page 20 for details.
- Logic AND gates should be used in conjunction with the SPWRGD signal to ensure voltage continuity from the voltage regulator at reset.

Hardware Implementation

Embedded system designs can be modified to support AMD PowerNow! technology with minimal design changes.

New traces must be added to route the new processor output pins to the proper hardware components. Based on the desired implementation of the AMD PowerNow! technology features, additional hardware may be required; and depending on the current system design, the voltage regulator may need to be updated to properly support AMD PowerNow! technology voltage transitions.

Figure 4 on page 19 illustrates an AMD PowerNow! technology design which uses the Maxim 1711 DC/DC regulator. Obviously, other devices can be used in exchange for those used in this example. Alternative components and matching input pins are provided in Table 8 on page 19.

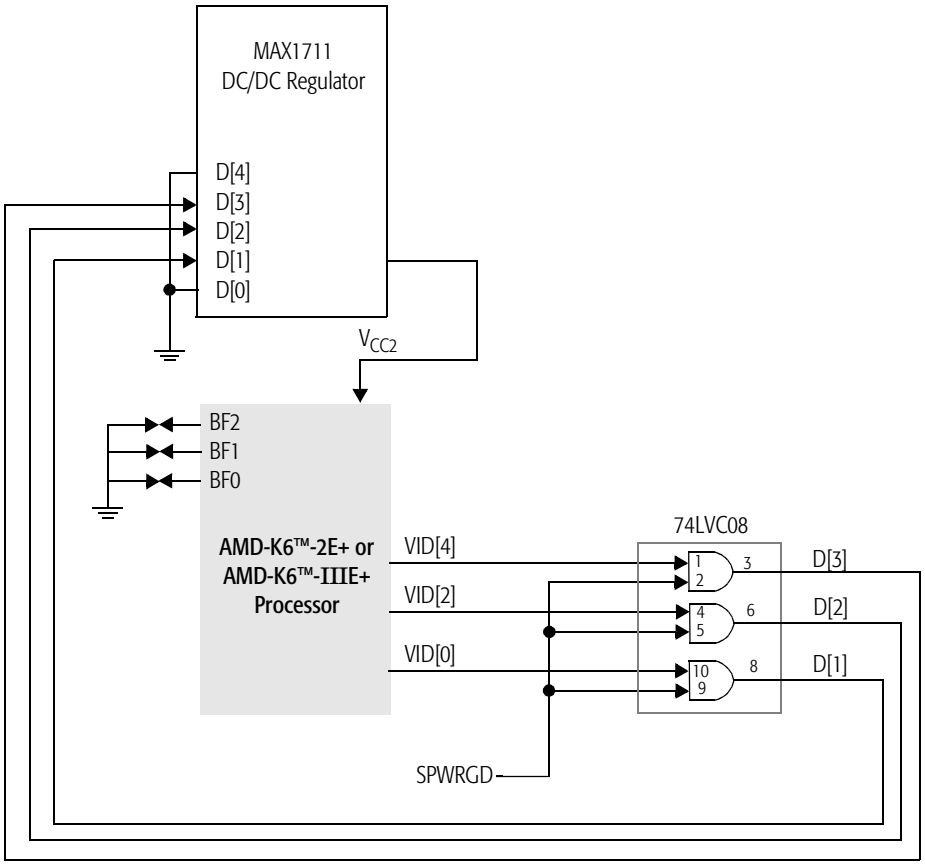

Figure 4. Example Hardware Implementation

Table 8. Alternative Components for AMD PowerNow!™ Technology Hardware Implementation

Component	Model and Input Pin Information				
DC/DC Voltage Regulator	Maxim 1711		Maxim 1714b		
	Pin Name	Pin No.	Pin Name	Pin No.	Comment
	D[4:0]	16-20	n/a	n/a	1714b does not use VID[4:0] inputs
	PGOOD	12	PGOOD	7	

Safe Voltage and Frequency Combination at Reset

A safe voltage and frequency combination at reset is a combination that provides functional processor operation conditions when RESET is negated.

Minimum Frequency Initialization

Systems that strap the processor BF[2:0] inputs to 100b configure the processor to boot with a core frequency of 2.0x the processor bus frequency upon RESET, which is the lowest supported frequency, are set for the *minimum* frequency initialization.

- The advantage to this implementation is that any supported AMD-K6-2E+ and AMD-K6-IIIE+ processor core voltage can be used for proper operation for the minimum frequency setting with the BF multiplier of 2.0x.
- The disadvantage of this method is that the maximum rated frequency of the processor cannot be determined by the state of the BF[2:0] pins.

Connecting the processor's VID[4:0] outputs to the regulator's D[4:0] inputs through a multiplexer that selects the processor's VID[4:0] outputs when SPWRGD = 1 will result in a CPU voltage of 1.5 V. If the processor's VID[4:0] outputs are mapped with a one-to-one correspondence to the regulator's D[4:0] inputs, it is required that the multiplexer drive 01010b to the D[4:0] regulator inputs, respectively, when SPWRGD = 0. This maintains V_{CC2} continuity at 1.5 V for the core voltage as SPWRGD transitions from unstable to good. The combination of 1.5 V and a 2.0x bus frequency multiplier provides a voltage and frequency at power up that guarantees functional operating conditions.

If the BF[2:0] inputs are strapped to select a 2.0x bus frequency multiplier, but a higher performance level is desired before loading the OS, then it is the responsibility of the BIOS or the RTOS to adjust the processor's core frequency and voltage to the desired operational level early in the POST routine.

Maximum Frequency Initialization (Recommended)

Systems that strap the processor BF[2:0] inputs so that the processor runs at the highest supported frequency are set for *maximum* frequency.

- The advantage of this implementation is that it does allow the BIOS to directly determine the CPU's maximum frequency by the state of the BF[2:0] pins.
- The disadvantage of this method is that it limits the number of regulator VID[4:0] input combinations and the output core voltage range available. It is also important to note that the V_{CC2} voltage will be initialized to 2.0 V.

If it is desired to have the processor run at its maximum frequency whenever RESET is asserted, all of the processor's VID[4:0] outputs cannot be tied directly to the regulator's D[4:0] inputs using this method. A total one-to-one VID[4:0] correspondence results in a core voltage supply of 1.5 V, which does not guarantee functional operation conditions at the processor's maximum frequency.

In the case that the BF[2:0] inputs to the processor are strapped to select the maximum CPU core frequency, additional logic is required to translate the CPU's default VID[4:0] output into a regulator input that is interpreted as a voltage that provides functional operation conditions at the processor's maximum frequency. The recommended solution is shown in Figure 4 on page 19.

For a step-by-step example of how to modify an existing design for this recommended implementation, see "VID[4:0] Modification for Maximum BF[2:0] Boot Option" on page 24.

Voltage Versus Frequency Options

In addition to initializing the processor at the minimum or maximum frequencies, intermediate frequency/voltage combinations can be selected, thereby allowing for additional flexibility in performance and power consumption.

Table 9 on page 23 and Table 10 list the minimum core voltage required to support various frequencies of a particular speed grade. For example, an AMD-K6-IIIE+ processor rated to run at 500 MHz at a nominal core voltage of 1.8 V is designed to run between 200 and 300 MHz with a nominal core voltage of 1.4 V.

Table 9. Supported Voltages and Operating Frequencies for Low-Power AMD-K6™-2E+ Processors Enabled with AMD PowerNow!™ Technology

Ordering Part Number[1]	Core Voltage	Range of Supported Operating Frequencies[2]	Active Power[3]
AMD-K6-2E+/450APZ	1.7 V	450–200 MHz	8.70–4.90 W
	1.6 V	400–200 MHz	6.90–4.20 W
	1.5 V	350–200 MHz	5.60–3.70 W
	1.4 V	300–200 MHz	4.30–2.95 W
AMD-K6-2E+/400xTZ	1.6 V	400–200 MHz	6.90–4.20 W
	1.5 V	350–200 MHz	5.60–3.70 W
	1.4 V	300–200 MHz	4.30–2.95 W
AMD-K6-2E+/350xUZ	1.5 V	350–200 MHz	5.60–3.70 W
	1.4 V	300–200 MHz	4.30–2.95 W

Notes:

1. *An x in this column represents the package type. See the processor data sheet for a full description of ordering part number notation.*
2. *AMD PowerNow! technology enables the operating frequency to step down in increments corresponding to the available bus frequency multipliers. Note that 250-MHz operation is not supported due to exclusion of 2.5 bus frequency multiplier.*
3. *Active application power dissipation for highest and lowest supported frequency at specified voltage.*

Table 10. Supported Voltages and Operating Frequencies for Low-Power AMD-K6™-IIIE+ Processors Enabled with AMD PowerNow!™ Technology

Ordering Part Number[1]	Core Voltage	Range of Supported Operating Frequencies[2]	Active Power[3]
AMD-K6-IIIE+500ANZ	1.8 V	500–200 MHz	11.40–5.80 W
	1.7 V	450–200 MHz	8.95–4.90 W
	1.6 V	400–200 MHz	7.10–4.20 W
	1.5 V	350–200 MHz	5.60–3.70 W
	1.4 V	300–200 MHz	4.30–2.95 W
AMD-K6-IIIE+450APZ	1.7 V	450–200 MHz	8.95–4.90 W
	1.6 V	400–200 MHz	7.10–4.20 W
	1.5 V	350–200 MHz	5.60–3.70 W
	1.4 V	300–200 MHz	4.30–2.95 W
AMD-K6-IIIE+400xTZ	1.6 V	400–200 MHz	7.10–4.20 W
	1.5 V	350–200 MHz	5.60–3.70 W
	1.4 V	300–200 MHz	4.30–2.95 W

Notes:

1. *An x in this column represents the package type. See the processor data sheet for a full description of ordering part number notation.*
2. *AMD PowerNow! technology enables the operating frequency to step down in increments corresponding to the available bus frequency multipliers. Note that 250-MHz operation is not supported due to exclusion of 2.5 bus frequency multiplier.*
3. *Active application power dissipation for highest and lowest supported frequency at specified voltage.*

VID[4:0] Modification for Maximum BF[2:0] Boot Option

The following section discusses a step-by-step process for modifying a design to accommodate the recommended maximum BF[2:0] boot option using the Maxim 1711 DC/DC voltage regulator. An assisting diagram is provided in Figure 5 on page 25.

- Disconnect processor output pins: AH32, AN35, R34, E25, and E17 from any current destinations
- Leave processor output pins AN35 and E25 unconnected
- Connect the Maxim 1711 DAC inputs D4 (pin16) and D0 (pin 20) directly to GND
- Add a 74LVC08 quadruple 2-input AND gate, connecting V_{CC} (pin 14) to +3.3V and GND (pin 7) to GND.
- Connect processor VID[4] (pin E17) to 74LVC08 pin 1
- Connect processor VID[2] (pin R34) to 74LVC08 pin 4
- Connect processor VID[0] (pin AH32) to 74LVC08 pin 10
- Add 10K-Ohm pull-up resistors on 74LVC08 pins 1, 4, 10 to +3.3V
- Connect SPWRGD (system power good) to 74LVC08 pins 2, 5, and 9
- Connect 74LVC08 pin 8 to Maxim 1711 DAC input D[1] (pin 19)
- Connect 74LVC08 pin 6 to Maxim 1711 DAC input D[2] (pin 18)
- Connect 74LVC08 pin 3 to Maxim 1711 DAC input D[3] (pin 17)
- Connect 74LVC08 pins 12 and 13 to GND to prevent the unused inputs from floating

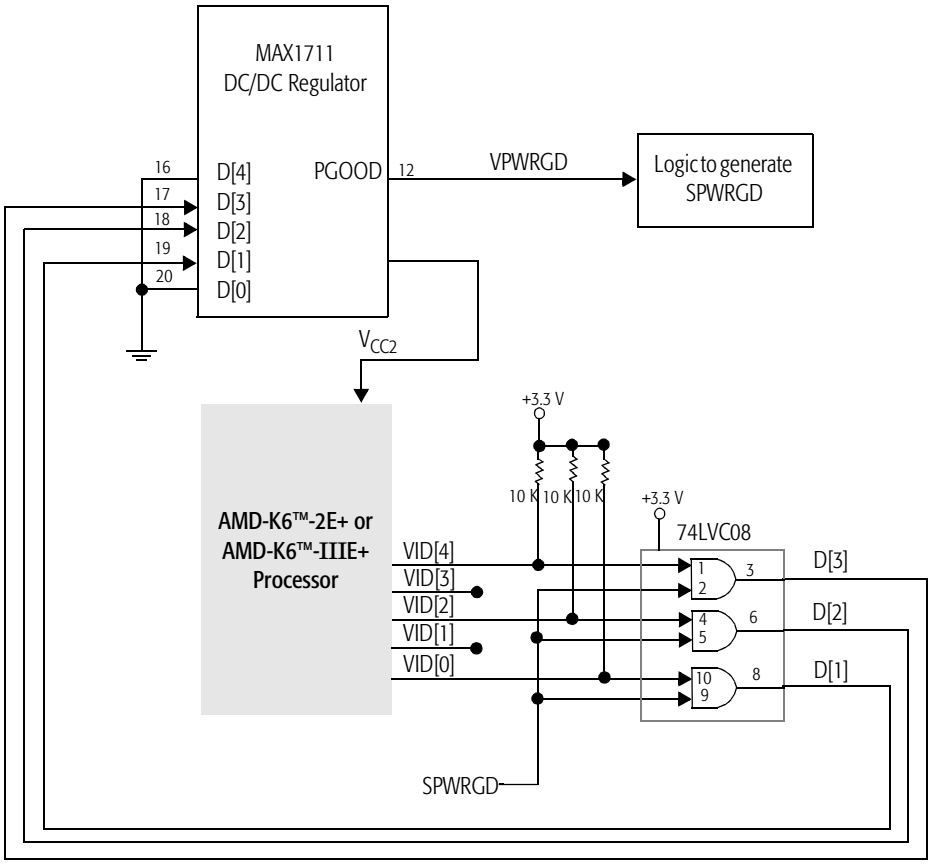

Figure 5. VID[4:0] Modification for Maximum Frequency Initialization

Gating PGOOD During a Voltage Transition

Most DC/DC regulators, such as the Maxim 1711, have an output to indicate a stable core voltage (PGOOD) that may glitch low during AMD PowerNow! technology voltage transitions. PGOOD can be used by system logic to generate the SPWRGD (system power good) signal. Because the south bridge asserts CPURST when SPWRGD is negated, any glitches of PGOOD during these state transitions must be intercepted in order to prevent a CPU reset.

The recommended solution for intercepting PGOOD and ensuring that a system reset does not occur during AMD PowerNow! technology core voltage transitions is to logically OR the PGOOD output with the PCIRST# signal. However, since the regulator's PGOOD signal is gated, this solution does not allow the system to monitor the CPU core voltage for guarding against an out-of-spec condition.

Figure 6 on page 27 illustrates the necessary modifications for intercepting the DC/DC regulator PGOOD signal AMD PowerNow! technology voltage transitions.

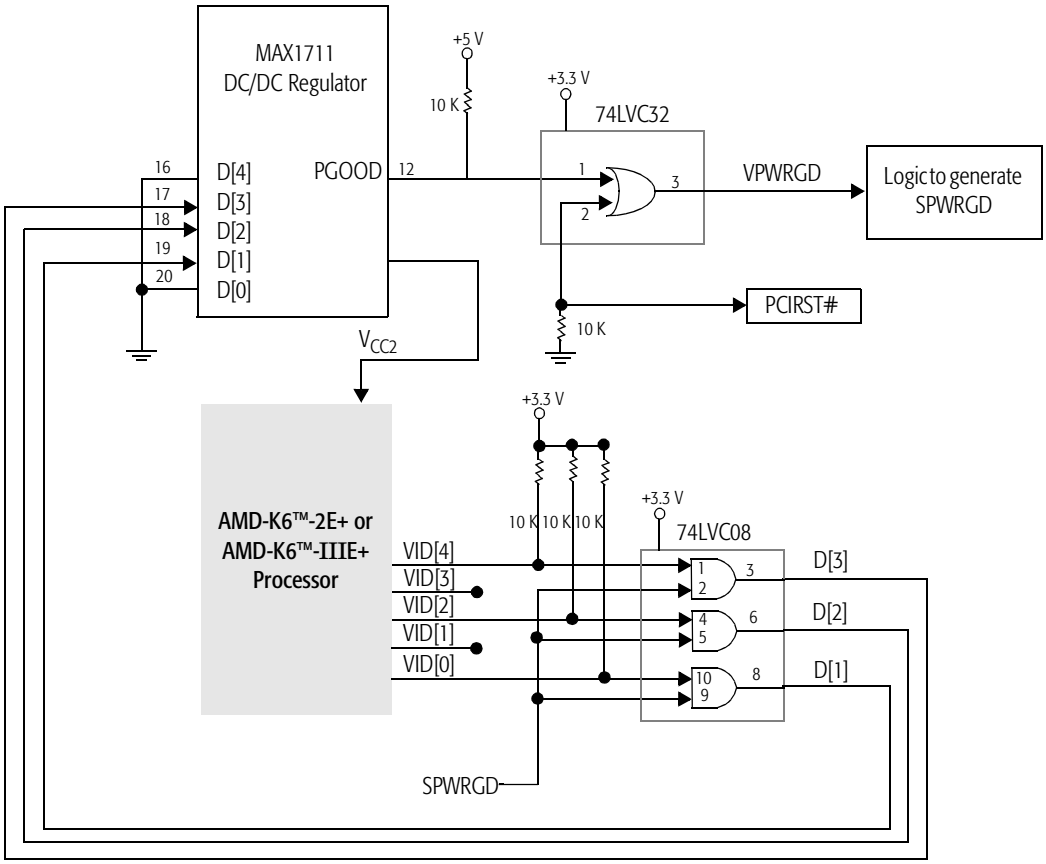

Figure 6. Gating the PGOOD Signal with Maximum Frequency Initialization

Software Implementation

CPU frequency and voltage setting combinations, called *AMD PowerNow! technology states*, are dependent upon a number of factors. The hardware design directly influences what states are available and supported in the system. These may be dependent upon performance preferences, power requirements or, most often, a combination of both.

Apart from the hardware design is the software implementation. How and what is implemented in software directly impacts when a state transition takes place and what voltage and frequency settings are invoked by the hardware.

Some software components that can be utilized to implement a fully ACPI-compliant power management scheme include:

- Real-time operating system (RTOS) enabled for AMD PowerNow! technology
- SMM handler
- Microsoft Windows® driver that supports AMD PowerNow! technology
- BIOS

Using an RTOS Enabled for AMD PowerNow!™ Technology

Some real-time operating systems supporting AMD PowerNow! technology will not require BIOS support or even a BIOS. In these instances, all the software required to invoke the EPM Stop Grant State and change the settings for voltage and frequency, or both, resides in the RTOS.

Using an SMM Handler

The AMD PowerNow! technology BIOS SMI API is the AMD-defined method for a driver to communicate with the BIOS in a Microsoft desktop operating system or with embedded Windows NT.

- If a driver is used, it will search for a BIOS-supplied table of information, which includes the address of the SMI command port.
- With the command port established, the driver then sets up parameters in general-purpose registers (the function and sub-function placed in the CX register) and generates an SMI by writing to the SMI command port.
- As the SMI command port mapping is specific to the south bridge, the BIOS/SMM developer must assign an eight-bit code to properly execute the SMM handler and enter SMM.
- Values are then returned in general-purpose registers, and SMM is entered.
- The driver can use "AMD PowerNow! technology BIOS calls" in SMM to invoke AMD PowerNow! technology state transitions, where these BIOS calls function in a similar manner to the BIOS INTn functions supported by Microsoft.

Using a Microsoft® Windows® Driver Supporting AMD PowerNow! Technology

The AMD PowerNow! technology-specific Microsoft Windows driver is the device driver that allows the communication of AMD PowerNow! technology preferences from the system to the BIOS or SMM code. Any BIOS that complies with the AMD PowerNow! technology BIOS SMI API specification is expected to support driver requests from any operating system or utility system that is able to make the proper calls.

The AMD PowerNow! technology driver also:

- Updates the memory table that is used to communicate user performance preferences to BIOS.
- Communicates system preferences or changes to the BIOS. This involves invoking the SMM handler (via the south bridge's SMI command port) when a state transition is desired.

Using a BIOS

The BIOS should contain the following:

- Table of AMD PowerNow! technology supported states used by the driver and SMM handler
- Data reflecting the current AMD PowerNow! technology settings
- The mapping information required by the driver to access the SMI command port in the system's south bridge.

AMD PowerNow!™ Technology Descriptor Table

The AMD PowerNow! technology descriptor table is a data structure typically built in the BIOS memory area at POST. It is used to convey information to an AMD PowerNow! technology enabled operating system kernel, device driver, or other interested application software.

After searching for, locating, and reading the table during initialization after POST, the AMD PowerNow! technology controlling software will have all the platform-specific information and will know how to access it through AMD PowerNow! technology control features.

The signature for the table is located on a 16-byte boundary in the area from 0x0C0000 to 0x0FFFFF or within the first 1 Kbyte of the extended BIOS data area.

Table 11 on page 31 provides the field definitions for the AMD PowerNow! technology descriptor table.

Table 11. AMD PowerNow!™ Technology Descriptor Table

Offset	Length	Description
0	4	Signature: "GBDT"
4	1	Length, in bytes, of the entire AMD PowerNow! technology BIOS descriptor table (no larger than 256 bytes.)
5	1	AMD PowerNow! technology BIOS API revision in BCD. Tens = major, Ones = minor
6	1	Checksum; entire table must sum to zero
7	1	Reserved
8	2	Bus speed in binary MHz (66, 75, 83, 92, 100, 112, 133, 150, 200, etc.)
10	2	Maximum CPU frequency for current processor in binary MHz
12	1	Maximum AMD PowerNow! technology state support by system ("N"). There are N+1 possible states and N<16. The minimum state is always zero.
		AMD PowerNow! Technology SMI Command Port Information
13	1	SMI Command Port Type/Size: Bit 0: Address Space, where 0 = x86 I/O address, and 1 = memory-mapped address. Bits 6–4: Data Size, where 001 = 8 bits (byte access), 010 = 16 bits, 100 = 32 bits. Bits 3–1, 7, and 8 are reserved and must be 0.
14	4	Address of SMI command port
18	4	AMD PowerNow! Technology_Code (Load ESI register with this number before making SMI call. Currently the code is defined as 9800_0089h.)
		Voltage/Frequency to State Map for Current System
22	2	State 0 CPU Voltage (A.BCD format)
24	2	State 0 CPU Frequency (in binary MHz)
26	1	State 0 VID[4:0]
27	1	State 0 BF[2:0]
28	2	State 1 CPU Voltage
30	2	State 1 CPU Frequency
32	1	State 1 VID[4:0]
33	1	State 1 BF[2:0]
34	2	State 2 CPU Voltage
36	2	State 2 CPU Frequency
38	1	State 2 VID[4:0]
39	1	State 2 BF[2:0]
xx	2	State N CPU Voltage
xx	2	State N CPU Frequency
xx	1	State N VID[4:0]
xx	1	State N BF[2:0]

Event Sequence for AMD PowerNow!™ Technology State Transitions

The following is a summary sequence of events outlining what must occur for a successful AMD PowerNow! technology state transition:

- An SMM handler or BIOS or operating system function may be called to carry out the AMD PowerNow! technology state transition.
- Set the ACPI-defined ARB_DIS bit in the north bridge to prevent PCI and AGP bus masters from being granted the bus and access to system memory while the AMD PowerNow! technology state transition is taking place. This is necessary because the processor is not capable of responding to cache snoops while its core voltage and/or frequency are being transitioned.

Note: *All bus activity to the processor must cease before initiating the AMD PowerNow! technology state transition. This is critical as a bus transaction may be in progress when the ARB_DIS bit is set. Additionally, there may be several memory accesses queued, which must be completed prior to entering EPM Stop Grant State.*

- Enable the EN bit of the EPMR register, making the frequency and voltage control fields accessible within the EPM 16-byte I/O block.
- Write the desired values for the requested operating voltage and frequency settings in the BVC field.
- Initiate the AMD PowerNow! technology state transition by writing a non-zero value to the SGTC field within the BVC field of the EPM 16-byte I/O block. This action causes the processor to enter the EPM Stop Grant state.
- After the AMD PowerNow! technology state transition, disable the EN bit of the EPMR register, which renders the frequency and voltage control fields invisible within I/O space.
- Clear the ARB_DIS bit in the north bridge to allow system memory accesses.
- If an SMM handler is used to invoke EPM Stop Grant State, a RSM instruction should be executed to return the CPU to normal operation.

Pinout Information

AMD-K6-2E+ and AMD-K6-IIIE+ low-power processors enabled with AMD PowerNow! technology use the AMD standard, 321-pin CPGA package and are also available in a 349-ball OBGA package.

To support AMD PowerNow! technology, five new output pins have been added that replace pins previously designated as either NC or INC pins.

Table 12 lists the new pins added to support AMD PowerNow! technology. Table 13 on page 34 and Table 14 on page 35 list the CPGA processor pins. Table 15 on page 36 and Table 16 on page 37 list the OBGA processor pins.

Table 12. Pins Added for AMD PowerNow!™ Technology

AMD PowerNow!™ Technology Function	Pin Name	CPGA Pin Number	OBGA Pin Number	Description
Voltage ID Control	VID[4]	E-17	A-11	These voltage identification outputs are used to drive the VID inputs of the DC/DC converter that generates the core voltage for the processor. The processor VID[4:0] outputs default to 01010b when RESET is asserted.
	VID[3]	E-25	C-15	
	VID[2]	R-34	L-19	
	VID[1]	AN-35	W-16	
	VID[0]	AH-32	W-17	

Table 13. CPGA Pin Designations by Functional Grouping

Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number
Control		**Address**		**Data**		**Data**	
A20M#	AK-08	A3	AL-35	D0	K-34	D52	E-03
ADS#	AJ-05	A4	AM-34	D1	G-35	D53	G-05
ADSC#	AM-02	A5	AK-32	D2	J-35	D54	E-01
AHOLD	V-04	A6	AN-33	D3	G-33	D55	G-03
APCHK#	AE-05	A7	AL-33	D4	F-36	D56	H-04
BE0#	AL-09	A8	AM-32	D5	F-34	D57	J-03
BE1#	AK-10	A9	AK-30	D6	E-35	D58	J-05
BE2#	AL-11	A10	AN-31	D7	E-33	D59	K-04
BE3#	AK-12	A11	AL-31	D8	D-34	D60	L-05
BE4#	AL-13	A12	AL-29	D9	C-37	D61	L-03
BE5#	AK-14	A13	AK-28	D10	C-35	D62	M-04
BE6#	AL-15	A14	AL-27	D11	B-36	D63	N-03
BE7#	AK-16	A15	AK-26	D12	D-32	**Test**	
BF0	Y-33	A16	AL-25	D13	B-34	TCK	M-34
BF1	X-34	A17	AK-24	D14	C-33	TDI	N-35
BF2	W-35	A18	AL-23	D15	A-35	TDO	N-33
BOFF#	Z-04	A19	AK-22	D16	B-32	TMS	P-34
BRDY#	X-04	A20	AL-21	D17	C-31	TRST#	Q-33
BRDYC#	Y-03	A21	AF-34	D18	A-33	**Parity**	
BREQ	AJ-01	A22	AH-36	D19	D-28	AP	AK-02
CACHE#	U-03	A23	AE-33	D20	B-30	DP0	D-36
CLK	AK-18	A24	AG-35	D21	C-29	DP1	D-30
D/C#	AK-04	A25	AJ-35	D22	A-31	DP2	C-25
EADS#	AM-04	A26	AH-34	D23	D-26	DP3	D-18
EWBE#	W-03	A27	AG-33	D24	C-27	DP4	C-07
FERR#	Q-05	A28	AK-36	D25	C-23	DP5	F-06
FLUSH#	AN-07	A29	AK-34	D26	D-24	DP6	F-02
HIT#	AK-06	A30	AM-36	D27	C-21	DP7	N-05
HITM#	AL-05	A31	AJ-33	D28	D-22	**Voltage ID**	
HLDA	AJ-03			D29	C-19	VID0	AH-32
HOLD	AB-04			D30	D-20	VID1	AN-35
IGNNE#	AA-35			D31	C-17	VID2	R-34
INIT	AA-33			D32	C-15	VID3	E-25
INTR	AD-34			D33	D-16	VID4	E-17
INV	U-05			D34	C-13		
KEN#	W-05			D35	D-14		
LOCK#	AH-04			D36	C-11		
M/IO#	T-04			D37	D-12		
NA#	Y-05			D38	C-09		
NMI	AC-33			D39	D-10		
PCD	AG-05			D40	D-08		
PCHK#	AF-04			D41	A-05		
PWT	AL-03			D42	E-09		
RESET	AK-20			D43	B-04		
SCYC	AL-17			D44	D-06		
SMI#	AB-34			D45	C-05		
SMIACT#	AG-03			D46	E-07		
STPCLK#	V-34			D47	C-03		
VCC2DET	AL-01			D48	D-04		
VCC2H/L#	AN-05			D49	E-05		
W/R#	AM-06			D50	D-02		
WB/WT#	AA-05			D51	F-04		

Table 14. CPGA Pin Designations for No Connect, Reserved, Power, and Ground Pins

Pin Numbers				
No Connect (NC)	**V_{CC2}**	**V_{CC3}**	**V_{SS}**	**V_{SS}**
A-37	A-07	A-19	A-03	AJ-27
C-01	A-09	A-21	B-06	AJ-31
S-33	A-11	A-23	B-08	AJ-37
S-35	A-13	A-25	B-10	AL-37
W-33	A-15	A-27	B-12	AM-08
AJ-15	A-17	A-29	B-14	AM-10
AJ-23	B-02	E-21	B-16	AM-12
AL-19	E-15	E-27	B-18	AM-14
Internal No Connect (INC)	G-01	E-37	B-20	AM-16
H-34	J-01	G-37	B-22	AM-18
Y-35	L-01	J-37	B-24	AM-20
Z-34	N-01	L-33	B-26	AM-22
AC-35	Q-01	L-37	B-28	AM-24
AL-07	S-01	N-37	E-11	AM-26
AN-01	U-01	Q-37	E-13	AM-28
AN-03	W-01	S-37	E-19	AM-30
Reserved (RSVD)	Y-01	T-34	E-23	AN-37
J-33	AA-01	U-33	E-29	
L-35	AC-01	U-37	E-31	
P-04	AE-01	W-37	H-02	
Q-03	AG-01	Y-37	H-36	
Q-35	AJ-11	AA-37	K-02	
R-04	AN-09	AC-37	K-36	
S-03	AN-11	AE-37	M-02	
S-05	AN-13	AG-37	M-36	
AA-03	AN-15	AJ-19	P-02	
AC-03	AN-17	AJ-29	P-36	
AC-05	AN-19	AN-21	R-02	
AD-04		AN-23	R-36	
AE-03		AN-25	T-02	
AE-35		AN-27	T-36	
		AN-29	U-35	
			V-02	
			V-36	
			X-02	
			X-36	
			Z-02	
			Z-36	
			AB-02	
			AB-36	
			AD-02	
			AD-36	
			AF-02	
			AF-36	
			AH-02	
			AJ-07	
			AJ-09	
			AJ-13	
			AJ-17	
			AJ-21	
			AJ-25	

Table 15. OBGA Pin Designations by Functional Grouping

Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number
Control		**Address**		**Data**		**Data**	
A20M#	W-4	A3	T-14	D0	H-18	D52	A-3
ADS#	U-1	A4	T-13	D1	G-19	D53	D-5
ADSC#	T-3	A5	W-15	D2	H-19	D54	C-3
AHOLD	K-4	A6	V-14	D3	F-17	D55	E-3
APCHK#	R-1	A7	U-14	D4	H-17	D56	D-2
BE0#	U-6	A8	T-12	D5	F-18	D57	E-4
BE1#	W-5	A9	W-14	D6	F-19	D58	D-3
BE2#	V-6	A10	V-12	D7	E-16	D59	D-1
BE3#	W-6	A11	W-13	D8	E-17	D60	E-1
BE4#	U-7	A12	W-12	D9	E-19	D61	F-3
BE5#	T-8	A13	U-13	D10	D-19	D62	F-2
BE6#	U-8	A14	W-11	D11	F-16	D63	F-4
BE7#	V-8	A15	U-12	D12	D-18	**Test**	
BF0	N-17	A16	T-11	D13	D-14	TCK	J-19
BF1	M-17	A17	W-10	D14	D-17	TDI	K-19
BF2	N-19	A18	V-10	D15	D-15	TDO	J-16
BOFF#	L-3	A19	U-10	D16	A-17	TMS	K-18
BRDY#	K-1	A20	T-10	D17	B-18	TRST#	K-17
BRDYC#	L-1	A21	T-17	D18	C-19	**Parity**	
BREQ	P-4	A22	T-19	D19	B-16	AP	R-3
CACHE#	J-4	A23	U-19	D20	A-16	DP0	G-17
CLK	U-9	A24	T-18	D21	D-13	DP1	C-17
D/C#	U-3	A25	V-18	D22	C-16	DP2	B-14
EADS#	V-4	A26	U-17	D23	A-15	DP3	C-11
EWBE#	K-3	A27	T-15	D24	C-14	DP4	C-8
FERR#	G-4	A28	R-16	D25	C-13	DP5	A-4
FLUSH#	T-7	A29	U-16	D26	A-14	DP6	C-1
HIT#	W-3	A30	V-16	D27	C-12	DP7	F-1
HITM#	U-4	A31	U-15	D28	A-13	**Voltage ID**	
HLDA	T-2			D29	A-12	VID0	W-17
HOLD	M-3			D30	B-12	VID1	W-16
IGNNE#	P-19			D31	D-11	VID2	L-19
INIT	P-17			D32	B-10	VID3	C-15
INTR	P-16			D33	A-10	VID4	A-11
INV	J-1			D34	D-10		
KEN#	K-2			D35	C-10		
LOCK#	T-1			D36	D-9		
M/IO#	J-3			D37	A-9		
NA#	L-4			D38	C-9		
NMI	R-17			D39	A-8		
PCD	R-4			D40	A-7		
PCHK#	P-3			D41	B-8		
PWT	V-2			D42	D-7		
RESET	W-9			D43	C-7		
SCYC	W-8			D44	B-6		
SMI#	P-18			D45	A-6		
SMIACT#	P-2			D46	C-6		
STPCLK#	M-18			D47	A-5		
W/R#	U-5			D48	D-6		
WB/WT#	M-2			D49	C-5		
				D50	C-4		
				D51	B-2		

Table 16. OBGA Pin Designations for No Connect, Reserved, Power, and Ground Pins

Pin Numbers				
No Connect (NC)	**V_{CC2}**	**V_{CC3}**	**V_{SS}**	**V_{SS}**
B-4	C-2	B-13	B-3	K-13
L-17	D-4	B-17	B-5	K-15
M-16	E-5	E-18	B-7	L-6
M-19	F-6	F-14	B-9	L-7
T-5	F-7	G-15	B-11	L-8
T-9	F-8	H-10	B-15	L-9
U-11	F-9	H-11	C-18	L-10
W-7	F-10	H-12	D-8	L-11
Internal No Connect (INC)	F-11	H-13	D-12	L-12
N-16	G-2	H-14	D-16	L-13
Reserved (RSVD)	G-5	H-16	E-2	L-14
G-1	H-4	J-15	E-6	L-16
G-3	H-6	J-18	E-7	L-18
G-16	H-7	K-14	E-8	M-5
H-1	J-5	L-15	E-9	M-12
H-2	K-6	M-14	E-10	M-13
H-3	K-7	N-15	E-11	M-15
J-17	K-8	N-18	E-12	N-2
K-16	K-9	P-11	E-13	N-6
M-1	K-10	P-12	E-14	N-7
N-1	K-11	P-14	E-15	N-8
N-3	L-2	R-10	F-5	N-9
N-4	L-5	R-13	F-12	N-10
P-1	M-4	U-18	F-13	N-11
P-8	M-6	V-11	F-15	N-12
R-8	M-7	V-15	G-6	N-13
R-19	M-8		G-7	N-14
	M-9		G-8	P-5
	M-10		G-9	P-7
	M-11		G-10	P-9
	N-5		G-11	P-10
	P-6		G-12	P-13
	R-2		G-13	P-15
	R-5		G-14	R-6
	T-4		G-18	R-7
	V-3		H-5	R-9
	V-7		H-8	R-11
			H-9	R-12
			H-15	R-14
			J-2	R-15
			J-6	R-18
			J-7	T-6
			J-8	T-16
			J-9	U-2
			J-10	V-5
			J-11	V-9
			J-12	V-13
			J-13	V-17
			J-14	
			K-5	
			K-12	

Documentation and Technical Support

The following documents provide additional information regarding the AMD PowerNow! technology initiative and the operation of the AMD-K6-2E+ and AMD-K6-IIIE+ processors:

- *Embedded AMD-K6™ Processors BIOS Design Guide Application Note* (order# 23913)
- *AMD-K6™-2E+ Embedded Processor Data Sheet* (order# 23542)
- *AMD-K6™-2E+ Embedded Processor Data Sheet* (order# 23543)

Appendix A—Frequently Asked Questions

New Output Pins

Question: What kind of output buffer do the new AMD PowerNow!™ technology output pins have?

Answer: The new processor output pins have standard CMOS "push-pull" driver buffers. All outputs are always driven.

Question: Are the new AMD PowerNow! technology output pins 5-V-tolerant?

Answer: No. The new AMD PowerNow! technology output pins adhere to the standard 3.3-V AMD-K6 family I/O voltage specification.

Question: What should be done for any AMD PowerNow! technology output pin that is not used?

Answer: Unused AMD PowerNow! technology output pins should be treated as NCs (no-connects).

AMD PowerNow!™ Technology State Transitions

Question: Are there any design limitations to voltage or bus frequency transitions?

Answer: Yes. System-initiated inquire (snoop) cycles are not supported and must be prevented during AMD PowerNow! technology transitions by setting the ARB_DIS bit in the north bridge.

Question: Is there a need to stop the CPU clock during state transitions?

Answer: No. However, state transitions must be performed while the processor is in the EPM Stop Grant State. The EPM Stop Grant state is a low-power, clock-control state entered by writing a non-zero value to the SGTC field for the purpose of changing the processor core frequency and voltage.

Question: Is there a need to assert RESET to perform AMD PowerNow! technology state transitions?

Answer: No. AMD PowerNow! technology state transitions are designed to operate dynamically and transparent to normal system operation.

Question: Are there any timing specifications for the length of a AMD PowerNow! technology transition period?

Answer: The suggested duration of time for a complete AMD PowerNow! technology transition is 200 μs.

Hardware Implementation

Question: If a maximum BF[2:0] boot strap option is implemented using the recommended AND-gate logic solution, is a multiplexer still required to guarantee a deterministic voltage at power on?

Answer: No. The AND-gate logic solution functions as a multiplexer. When the system power good (SPWRGD) signal is Low, the AND-gate logic drives the regulator inputs appropriately. When SPWRGD is High, the AND-gate logic allows the processor VID[4:0] outputs to drive the regulator inputs.

Question: Can a signal other than the SPWRGD be used for gating the CPU VID[4:0] outputs?

Answer: Yes, the PCI reset pin can also be used to gate the CPU VID[4:0] outputs to the DC/DC regulator. However, the system must ensure that PCIRST# is driven low when power is applied to the processor.

Software Implementation

Question: If the BIOS needs to access the EPMR register during POST before the SMM handler is installed, can the EPMR register be accessed outside of SMM?

Answer: Yes. However, the SMM handler must be installed before SMIs initiated by AMD PowerNow! technology can be serviced.

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