IEEE 1394: Status and Growth Path

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[Gerald Marazas, 1394 working-group chair and a senior engineer in the IBM PC Company's Architecture Department, submitted this update on IEEE Std 1394-1995 High Performance Serial Bus. He describes the standard's current status in industry and enumerates possible extensions for second-generation standardization. For further details on Std 1394, see "P1394: Good for desktops and portables," Micro Standards, April, 1995.S.L.D.]

In December 1995, the final public review of the High Performance Serial Bus draft standard concluded, and the IEEE ratified it as IEEE Std 1394-1995. As 1394 working-group chair, I extend my appreciation to all those who took the time to review, vote, and comment upon the draft standard. It is also gratifying to the entire working group to observe the various computer and digital audiovisual (AV) products now incorporating support for the 1394 interface.

This column's purpose is to review technical issues raised by the IEEE study group exploring the development of a second-generation standard based on 1394. This second-generation activity is likely to consist of several 1394-related working groups, each expanding a different attribute or capability of the standard. To set a proper foundation for the discussion of 1394's future, I first summarize the concepts and facilities of the present standard and review its current status in the computer and digital AV industries.

Environments

Std 1394 defines two physical environments: cable and backplane. Because the cable environment currently generates more activity in terms of second-generation standards development, I focus on it here.

The cable environment defines 1394 as a high-speed, low-cost, serial data bus, suitable for connecting computer peripherals and digital AV devices to each other as well as to computer systems. Its specified data transfer rates are 98.304, 196.608, 393.216, and 786.432 Mbits per second. The backplane environment defines 1394 as a low-cost, serial bus backup to parallel data backplane buses. The specified data transfer rates in this environment are 24.576 and 49.152 Mbps. All six of these data rates are integer multiples of both the ISDN basic rate and the data rates of several communications systems.

Protocol stack

The protocol stack in Figure 1 depicts the major components of a full-function 1394 node. A minimum-function (repeater) node contains only the physical-layer component. Nodes involved in 1394 applications activity contain the additional components shown in Figure 1. The physical layer supports attachment to the 1394 physical media. Supported functions include electrical signaling, arbitration, and definition of mechanical interfaces. The link layer supports packet layer functions such as addressing, data checking, and data framing. The link layer also supports two data transfer modes—asynchronous and isochronous—described later.

The transaction layer supports a complete request-response protocol for read, write, and special lock operations as described in IEEE Std 1212-1991 Control and Status Register (CSR) Architecture. Figure 1 depicts the transaction layer box as narrower than the protocol stack's other elements to convey the notion that the isochronous data transfer mode bypasses the transaction layer. Isochronous data transfers involve direct exchanges between the application and link layers. Asynchronous-mode data transfers, however, require services of the link layer. The application layer denotes one or more applications using 1394 services provided by the lower layers in the protocol stack.

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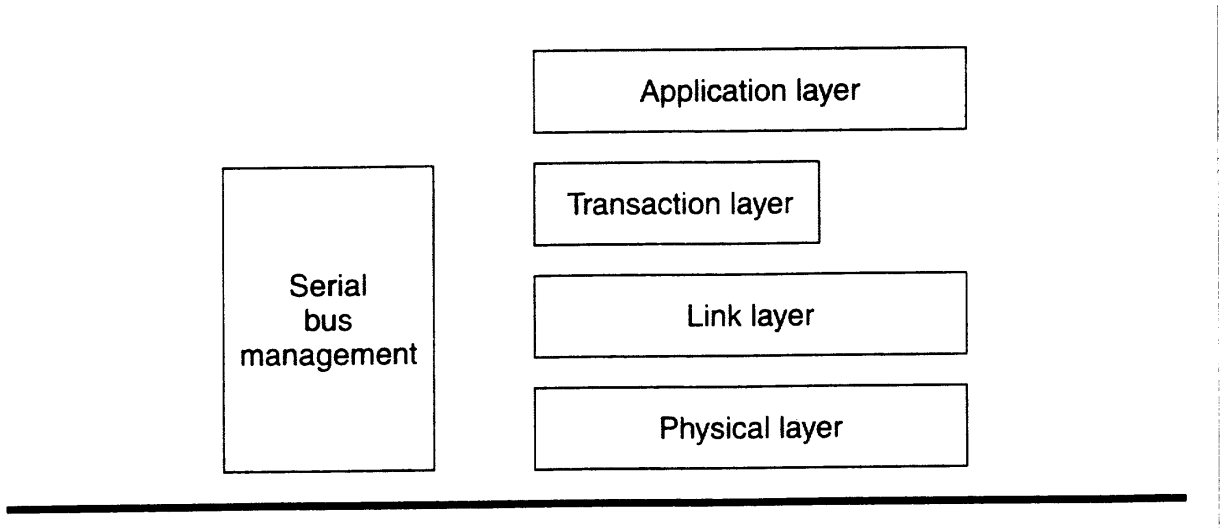

Figure 1. IEEE Std 1394 protocol stack.

Figure 1 shows the serial bus management component to the left of the protocol stack. Bus management interacts with the physical, link, and transaction layers, as well as with the application layer. The two 1394 physical environments share the same logical protocol at the link and transaction layers. They also share the definition of data transfer in an optional isochronous mode and a required asynchronous mode.

Today, cable environment implementations of 1394 involve a distinct physical chip and a separate link chip. These environments generally implement the remaining components of Figure 1 in software. In the near future, cost-reduced 1394 implementations will integrate physical and link functions on a single chip.

In addition, future implementations may integrate 1394 silicon functions into a chip that also supports non-1394 functions at a given node. The chip integration process may also entail a change in speed signaling the way a physical component capable of data transfer at two or more rates indicates which data rate it will use for a given packet transmission.

Data transfer modes

Data transfer via the asynchronous mode consists of nonscheduled, acknowledged delivery of data packets over the 1394 bus. A packet proceeds from a single source node to a specified address in the address space of a single, specified destination node. While there is no guarantee of latency (bandwidth) for asynchronous transfers, the 1394-defined fairness protocol allows for equitable division of available asynchronous bandwidth.

In the isochronous mode, data transfer consists of scheduled, nonacknowledged delivery of data packets over the bus. A 1394-defined isochronous resource manager allocates available isochronous bandwidth among originators of isochronous data. In this mode, a packet proceeds from a single source node via transmission on an assigned isochronous channel number. There may be zero, one, or multiple nodes receiving isochronous data on that channel. Isochronous data transfers have a guaranteed, bounded worst-case latency.

The two physical environments share the same definition of the structure for 1394's 125-ms time cycle. According to this definition, 1394 cycles occur at an ISDN-friendly, 8-KHz rate. The 1394 cycle structure divides cycles into an optional isochronous data transfer portion and a required asynchronous portion. Any 1394 bus that supports isochronous data transfer must include a node acting as isochronous resource manager. This resource manager coordinates use of isochronous bandwidth and channel number by 1394 nodes originating isochronous data packets. Even within a system engaging exclusively in isochronous applications, however, the standard sets aside 20 percent of total bandwidth for the asynchronous data transfer mode. This reserved bandwidth allows applications and resource management to send various control packets that require the asynchronous mode.

Isochronous data transfer typically proceeds such that the system does not use the full allocation of isochronous bandwidth on each cycle. Std 1394's facility of making unused isochronous bandwidth available for asynchronous transfer enhances efficient bus operation.

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Address space model

Figure 2 shows the structure of the 64-bit addresses used by all nodes in the two 1394 physical environments. The 64-bit, open memory map model (per the CSR architecture) is one of the key and characterizing features of a 1394 system. (Interested readers should refer to IEEE Std 1212-1991 CSR Architecture for details. To order this standard or the IEEE Standards Catalog and Supplements, call (800) 678-IEEE or e-mail k.mccabe@ieee.org.)

A 1394 system may, in principle, consist of a universe of up to 1,023 individual 1394 buses interconnected by a suitable collection of bus bridges. As depicted in Figure 2, within a 1394 address, the high-order 10 bits specify the bus number (bus_ID) for up to 1,023 individual buses. The adjacent 6 bits specify the physical ID (phy_ID) that distinguishes a given node among up to 63 nodes connected to any given 1394 bus. The remaining 48 bits define byte addresses available for use by any given node on a particular 1394 bus.

This universe of interconnected 1394 buses and nodes has a common 64-bit address space shared by all nodes. A powerful feature of the 1394 address model is that, without constraints being imposed, each node has access to the memory addresses of all nodes in its universe. This model permits efficient distribution of the DMA context to the peripheral nodes. The DMA context includes the DMA engine, control parameters, and target buffer address that a peripheral node uses to make read or write access to addresses in another node in the 1394 universe. This model contrasts with that of many traditional systems, in which the DMA context is closely held in a central or host system.

A significant benefit from the 1394 approach is efficient, peer-to-peer data transfer between interconnected 1394 nodes. However, some users of systems that include 1394 peripherals have raised concerns about security and privacy. Commercial users in particular will be interested in the potential security and privacy enhancements to 1394 described later.

1394 physical architecture

Within the cable environment, the external-device interconnect specification defines six leads. Four leads provide a data- and strobe-signaling scheme implemented over two differential pairs. Clocking may be recovered from an exclusive-OR operation upon the two signals. Clearly, the signaling scheme is not DC balanced. However, advantages of the approach are its low cost and excellent ability to tolerate phase jitter between the data and strobe signals.

The remaining two leads support cable and ground. The 1394 ability to provide cable power assures that the system meets the requirement that the physical layer be in a power-on state for all nodes interconnected on the same 1394 bus. In this manner, the system guarantees that all nodes are “visible” during the self-configuration process occurring after 1) initial power-on and 2) addition of a new node or removal of a node from an existing 1394 system. Because of this visibility during self-configuration, the system automatically assigns each node a unique address (phy_ID). Without cable power, each node must power to its physical component, even when that node appears to the user to be in a power-off state.

Digital AV equipment manufacturers have implemented a different cable and connector in their 1394 products. Power and ground needs in consumer-oriented digital AV equipment are sufficiently different that the last two leads are not necessary. Thus, these manufacturers implement the 1394 interface with only four leads, supporting the two-differential-pair, data and strobe signal scheme as specified in the standard. This four-lead implementation is smaller than the standard’s six-lead specification.

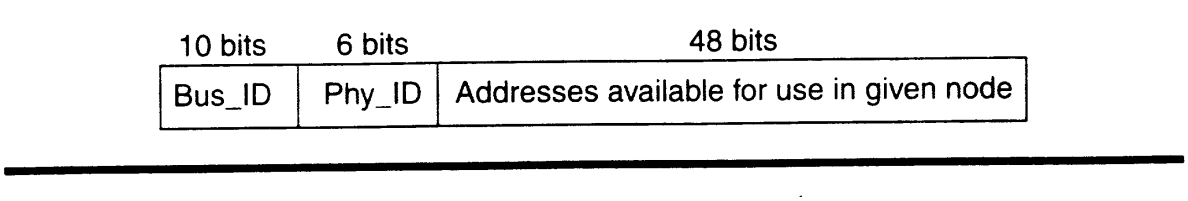

Figure 2. Structure of 64-bit address used by 1394 nodes.

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Unregulated DC power of up to 60W may be supplied via the cable system. As specified in the 1394 standard, a node supplying cable power may/must provide up to 40 volts and up to 1.5A. The standard restricts permissible voltage drop to one volt in the cable connecting two nodes. Taking into account the maximum diameter allowed cable wires, the maximum distance between two nodes is 4.5 meters. If signal detectability rather than voltage drop were the criterion, two connected 1394 nodes could be up to 10 meters apart.

The 1394 interconnect architecture supports a very rich topology. Nodes equipped with two ports may connect in daisy chain fashion; those with three or more physical ports may connect in a general tree structure. In all cases, the standard permits no closed loops. As a consequence, there must be only one path between any node and the arbitration root. The farthest apart nodes may be separated by up to 16 hops (16 physical connections), yielding a maximum distance of 72 meters. In a 1394 system containing a bus manager node, optimization of arbitration time occurs to yield optimum throughput results for the given system of interconnections.

Industry status

Since the standard's ratification, leading computer and digital AV companies have expressed their intention to support 1394. Apple Computer, Compaq, Digital Equipment, IBM, Microsoft, Sony, Sun Microsystems, and Texas Instruments have all voiced interest in the interface. A common theme is the high desirability of connecting the new world of digital AV equipment to personal computer systems. These companies believe that such connectivity is critical to applications with which users manipulate, interact with, and display digital AV data on computer systems.

Another theme in the public statements is interest in using the high-speed, serial data 1394 bus to replace present parallel data I/O buses such as IDE and SCSI. Analysts observe that 1394's isochronous transfer mode need not be used in every device or system implementation. They argue that reliance on 1394's asynchronous transfer mode alone provides a very effective mass storage interface for desktop and mobile computer systems.

Clearly, 1394's asynchronous mode accomplishes traditional computer applications undertaken today with parallel-data, asynchronous I/O buses. It also achieves worthwhile performance levels for computer-based AV applications. Isochronous-mode 1394 broadens the scope and increases performance in terms of more frames per second and higher video resolution for computer-based AV applications.

For today's personal computers with multitasking operating systems, observers note 1394's ability to overlap (interleave) multiple concurrent I/O commands. The 1394 overlap operation and peer-to-peer data transfer capability provide significant performance and functional benefits. As viewed by advocates, significant cost savings result from serial packaging coupled instead of IDE parallel bus packaging. The near-term emergence of 400-Mbit 1394 implementations will enhance expandability and performance growth. Advocates further note the 1394 winning combination gets even better with the appearance of 800-Mbps implementations.

Other 1394 observers would like to address various system integration considerations. Computer security and privacy rank high among factors needing careful implementation. While 1394 may not pose a greater security risk than SCSI, there is currently a high sensitivity to security topics in all data-processing situations.

For 1394, the focus is upon the open nature of the address model. There is concern in exposing the entire area of host memory to the outside world of an external I/O bus. One implementation proposal addresses this concern by restricting 1394 I/O access to certain defined buffer areas in host memory. Hardware support in the host would act to reject memory accesses directed to any address outside the identified buffer areas. Other proposals involve use of a digital token, perhaps combined with the notion of a preview buffer to certify legitimacy of a given I/O operation.

An asynchronous stream is still another proposal for enhancing 1394 security and privacy. An asynchronous stream is similar in concept to today's isochronous stream. Host memory addresses would be kept private from external devices, which would use only a newly defined asynchronous-stream channel number. In this proposal, host hardware would direct asynchronous stream data received on a given channel number to an appropriate area of host memory.

Future standardization areas

An IEEE-approved committee has been meeting to formulate recommendations for second-generation extensions to Std 1394. The committee expects that one or more 1394-based projects will be approved, so that working groups may form and standards development begin.

One consideration in the proposed extensions is the view of 1394 as a special-purpose network appropriate for use in a home or a small office building. Another possible vision for 1394 is its extension for use in high-performance, mass storage systems.

The special-purpose network view of 1394 would involve a number of possible extensions. Hardware

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technology is close at hand both to extend the distance and increase the data transfer rate of 1394 operation. Representatives from several companies indicate gigabit operation for 1394 is feasible as well as desirable.

Physical-media changes are highly likely as 1394 operation extends to one gigabit and beyond. Many of us believe the standard needs a DC-balanced signaling method. Other proposed changes involve a new approach to bus arbitration and possible full-duplex operation. Through all these possible physical-level changes, we expect transaction level operation of the new 1394 to remain compatible with 1394-1995. Thus, 1394 applications and other software can remain the same across these contemplated hardware changes. There is also the expressed demand for the new 1394 to remain a low-cost serial bus, scalable to still higher data transfer rates as technology continues to evolve.

Another change under consideration is a substantial increase in single-hop distances between adjacent nodes from today's 4.5-meter limit. Some seek single-hop distances of at least 25 meters; others argue for a capability of 100 meters or more. Cable power would probably not be distributed over these longer hops. This area of change supports the notion of using the new 1394 as a backbone facility to connect some number of subnets involving the lower speed (800-Mbit) 1394-1995.Another change under consideration is a substantial increase in single-hop distances between adjacent nodes from today's 4.5-meter limit. Some seek single-hop distances of at least 25 meters; others argue for a capability of 100 meters or more. Cable power would probably not be distributed over these longer hops. This area of change supports the notion of using the new 1394 as a backbone facility to connect some number of subnets involving the lower speed (800-Mbit) 1394-1995.

Another possible change is to incorporate the means to detect and electrically disconnect alternate paths between two given 1394 nodes. In today's 1394, alternate paths between nodes are not possible; multipathing would imply the presence of the prohibited loop connection between the nodes. However, allowing alternate paths would give 1394 the ability to support high-availability concepts in modern, mass storage systems.

With the proposed capability, multipath connections could be wired between selected nodes. As appropriate, the alternate paths would remain in place physically but would be electrically disconnected. Thus, in operation, there would be one and only one electrically active path between nodes. Should a presently activated path fail for some reason, the mass storage system could continue to operate by deactivating the failed path and reactivating an appropriate alternate path. The combination of gigabit data transfer capability and high availability would make the new 1394 an interesting possibility for RAIDS (redundant array of inexpensive disks) and other high-performance mass storage systems.

Still another possible extension to 1394 is the explicit definition of bus bridges in a 1394 network. Clearly, one use for a bus bridge is to connect a 1394-1995 bus with its present physical media to a new 1394 bus operating in terms of new (gigabit and/or long-distance) physical media. A bridge is also appropriate for systems composed entirely of 1394-1995 buses, where the bus bridge(s) would isolate traffic on one bus from another. The bridge need only transfer the fraction of total traffic intended to flow from one bus to the other. In this way, the collection of bridged 1394 buses could accommodate an aggregate of traffic much higher than is feasible for any single 1394-1995 bus.

In light of this present and proposed activity, 1394 clearly has a most interesting and highly promising role in personal computer and digital AV systems. I encourage all interested parties to join the next wave of 1394 product and standards development. The scope and future of 1394 is rapidly expanding.

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