AMD

AMD-K6™ Processor

Microarchitecture Overview
and
Product Update

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Agenda

AMD

- Microarchitecture Overview
- Silicon Technology
- Summary

Design Basics

- Decoupled Decode/Execution Superscalar x86 Processor
- Instruction Predecoding
- Large Level-One Caches
- Multiple Sophisticated Decoders
- Out-of-Order Execution Engine
- Centralized Instruction Control Unit
- Specialized Parallel Execution Units
- Binary Compatible MMX Multimedia Unit
- Socket 7 Compatible

Internal Block Diagram

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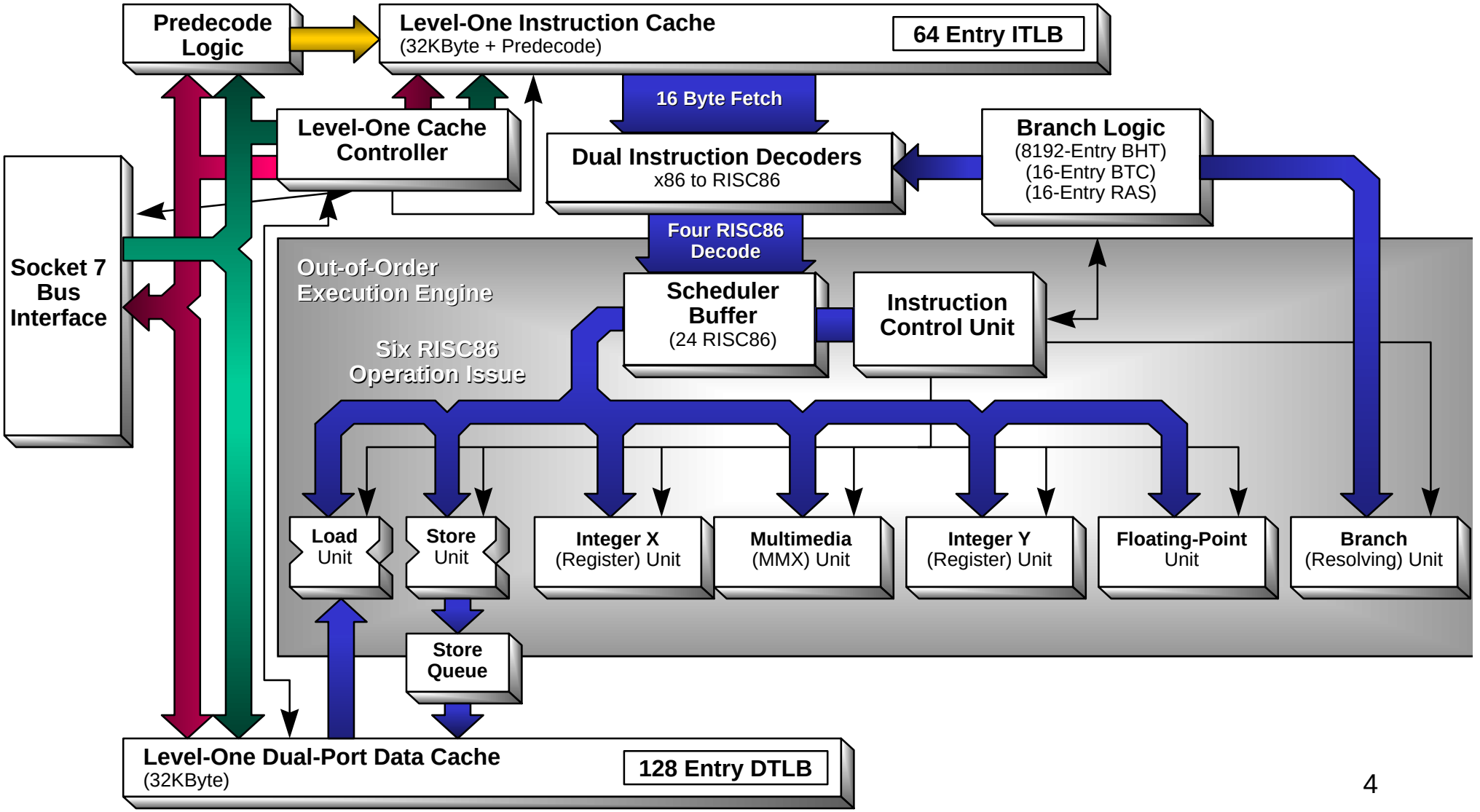
AMD-K6™ Processor Microarchitecture Overview



AMD-K6 DIE Photograph

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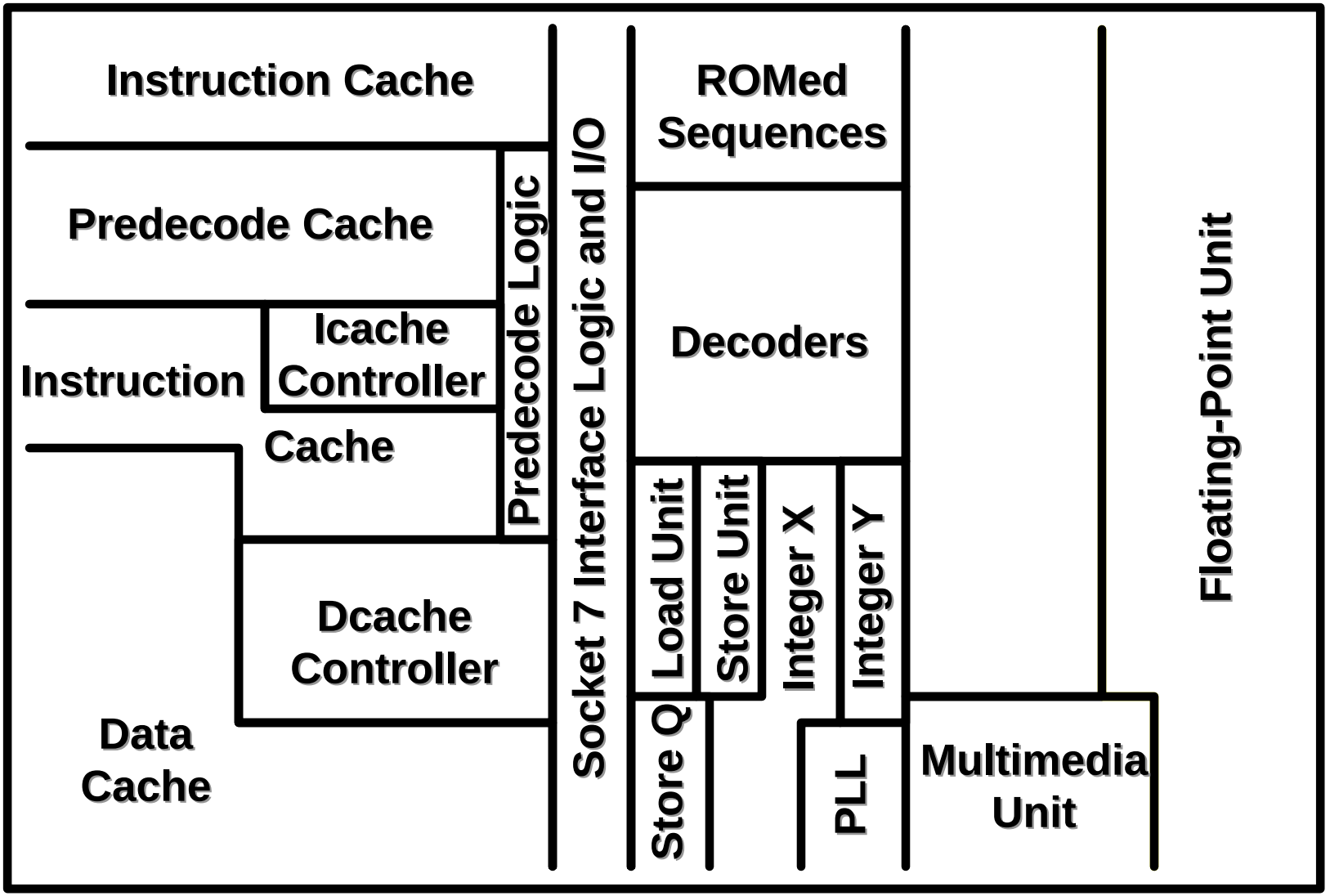
AMD-K6™ Processor Microarchitecture Overview

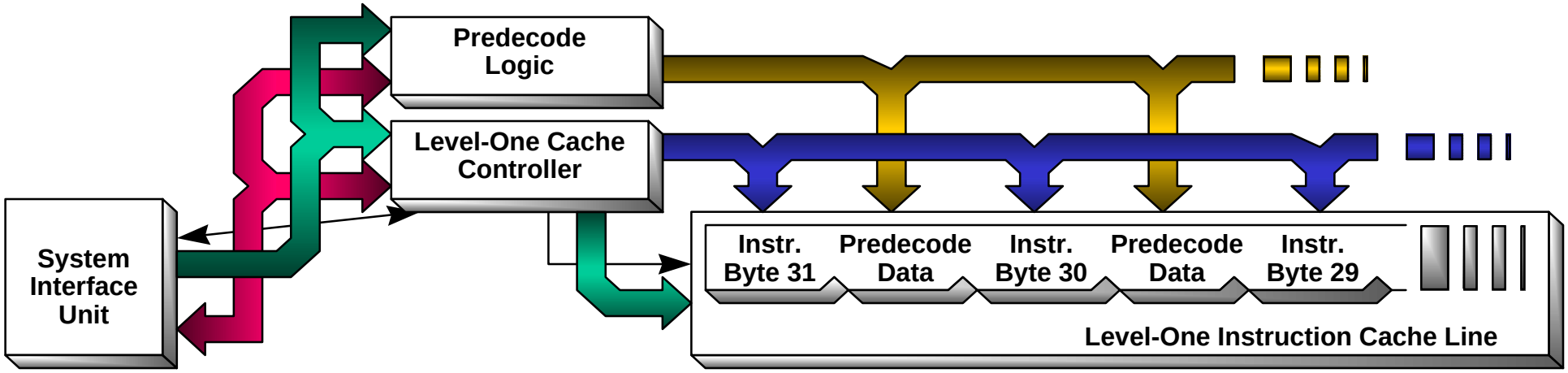


Front End - Level One Caches

- **Split Level-One On-Chip Caches**
- **Instruction Cache**
  - 32K Byte in size
  - 2-Way Set Associativity
  - 32 Byte Line Size
  - Single Cycle Access
- **Dual Port Data Cache**
  - 32K Byte in size
  - 2-Way Set Associativity
  - 32 Byte Line Size
  - Write-Back Policy
  - Supports simultaneous loads and stores in a Single cycle
  - Full MESI support

Front End - Predecode Logic

- Predecoding allows higher sustainable decode bandwidth!
- Identifies Instruction Boundaries for Decoders
- Decoding begins during level-one instruction cache fills
- Predecode data stored along side the L1 Instruction Cache
- Instruction lengths determined on a byte by byte basis



Front End - Decoders

◆ Sophisticated x86 Decoders

- Direct hardware translation for most x86 Instructions
- Most x86 Instructions decode as 1 to 4 RISC-like operations

◆ Dual Short Decoders

- Decodes up to two x86 instructions per clock
- Decoders supports translation of the most commonly used x86 instructions
- Short Decoders can generate up to two RISC86 operations each

◆ Long Decoder

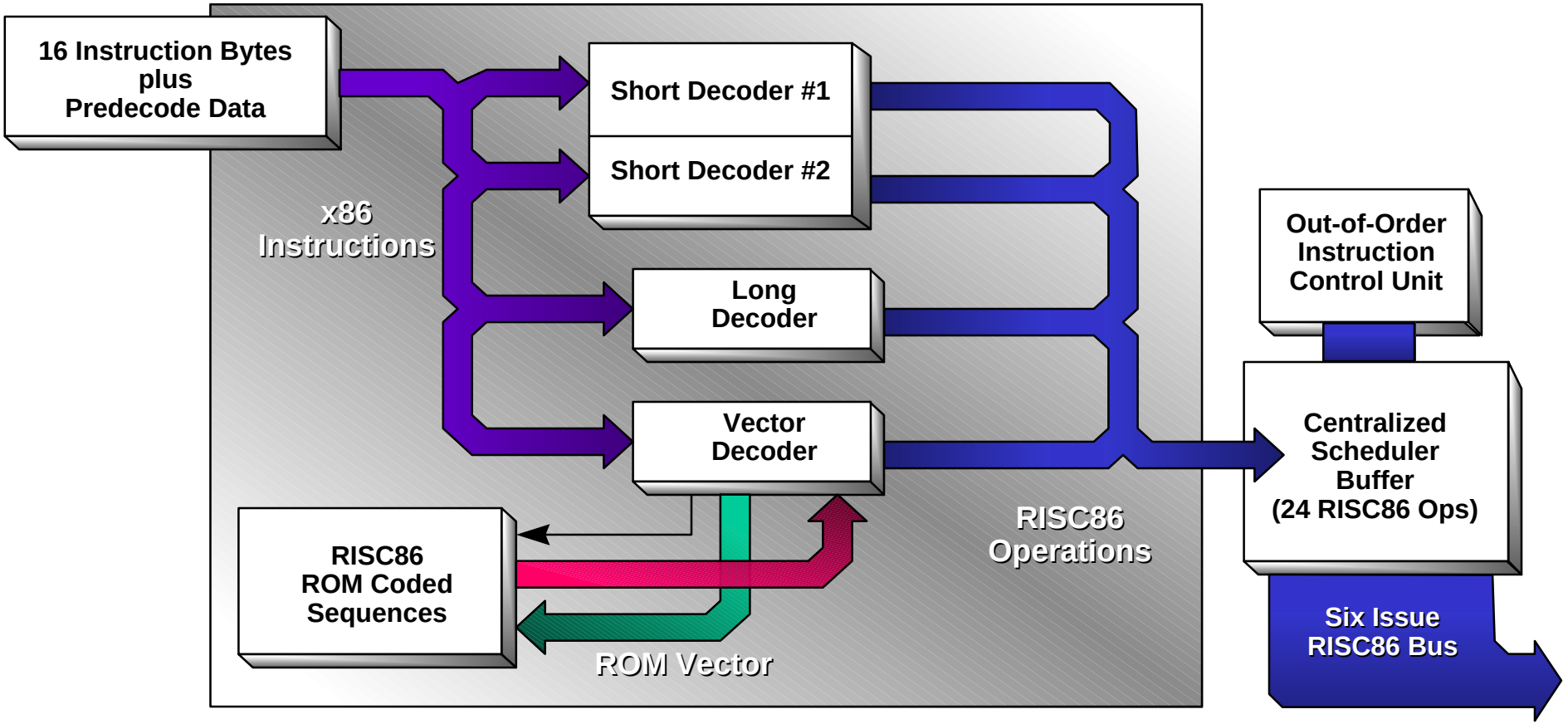
- Decodes semi-common and commonly used x86 instructions
- Generates up to four RISC86 operations

◆ Vector Decoder

- Uncommon, complex code is mapped into ROM-resident RISC86 sequences
- Generates the first set of RISC86 operations and a ROM vector

Front End - Decoders

- **Block Diagram of Sophisticated x86 Decoders**



Six Issue Out-of-Order Engine

- **Instruction Control Unit**
  - Centralized Scheduler Buffering up to 24 RISC86 Operations
  - Full register renaming (48 total Registers)
  - Full out-of-order issue and speculative execution
  - Six RISC86 issue and In-order retirement
- **Seven Parallel Execution Units**
  - Two Stage Load and Store units
  - Integer X, Integer Y, Floating-Point and Branch units
  - Intel MMX instruction compatible Multimedia unit
- **Branch Logic**
  - Two-Level Branch Prediction based on 8192-entry Branch History Table
  - Target address calculation occurs during decode cycle
  - 16-entry Branch Target Cache
  - 16-entry Return Address Stack

AMD-K6™ Silicon Technology

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- **Designed for AMD Scaleable 0.35 Micron Process**
- **Transistor Channel Length 0.3 Micron**
- **Shallow Trench Isolation (Low Junction Capacitance)**
- **Design Scaleable to 0.25 Micron process**
- **Six Total Interconnect Layers**
  - Local Interconnect (level - 0)
  - 5 Global Interconnect or metal layers
- **C4 Technology for flip-chip mounting**
  - Low inductance for I/O signals
  - Improves power distribution and die size
- **Contains 8.8 Million transistors**

Feature Summary

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AMD-K6™ Processor Advantage

	AMD-K6	Intel Pentium Pro
x86 Decoders	2 Sophisticate, 1 long, 1 vector	1 Sophisticated, 2 simple
Decode Bandwidth: 32-bit typ/max	1.9/2.0	2.1/3.0*
Decode Bandwidth: 16-bit typ/max	1.8/2.0	1.5/3.0*
Average RISCops/x86: 32-bit code	1.2 (lower is better)	1.5*
Average RISCops/x86: 16-bit code	1.5 (lower is better)	2.0*
Maximum ROp Issue Rate	6	5
Speculative Execution	Yes	Yes
Out of Order Execution	Yes	Yes
Physical Registers	48	40
Centralized Buffer max/active	24/18	40/20
FPU Multiply/ADD Latency	2/2	5/3
Pipeline Stages	6	12
Misaligned Loads	1 cycle penalty	6 cycle penalty
Branch History Table	8192 entries	512 entries
Branch Prediction Accuracy	95%	85-90%
Misprediction Penalty	1-4 (Short Pipeline)	10-15 cycles
Instruction/Data TLB	64/128 entries	32/64 entries
L1 Instruction-Cache	32KB +Predecode 2-Way Set-Assoc.	8KB 2-Way Set-Assoc.
L1 Data Cache	32KB, 2-Way Set-Assoc. (Load+Store)/cycle	8KB, 4-Way Set-Assoc. (Load+Store)/cycle
Local Bus Bandwidth	528 MB/sec	528 MB/sec
Local Bus Latency	2 clocks	5-7 clocks

*** "Nx686 Goes Toe-to-Toe with Pentium Pro", Microprocessor Report, Vol.9 No.14, Oct. 23, 1995, MicroDesign Resources**

Conclusion

AMD

- Leading Edge 6th Generation Architecture with MMX Technology
- State of the Art .35 micron, 5 layer metal Process Technology
- Low-Cost, High Performance Socket 7 Infrastructure
- World class FAB 25 sub-micron Manufacturing Capability