Rambus and Direct DRAM

Intel's Solution to the "Insatiable need for Memory Bandwidth"

March 1997

Rambus Memory Systems

The Platform Design Perspective

- Masters and slaves are coupled to the ***Rambus Channel*** via a ***Rambus Interface***
- The memory controller (a prototypical master) is designed to the Rambus Channel specs, not for specific DRAMs (or other slaves)
- Rambus DRAM (***RDRAM***, the prototypical slave) are expected to meet Rambus Channel specs for timing and pinout
- RDRAMs have high bandwidth with small packages and pin count relative to other DRAM technologies

Rambus Bandwidth

- Due to single-byte width, burst transfer rate in MB/sec is equal to the internal clock rate in MHz
  - On-chip clock rate of latest “Concurrent RDRAM” is twice the external clock
- 100MHz/year internal clock ramp
- Bandwidth Roadmap
  - 500 MB/sec in ‘95
  - 533 MB/sec in ‘96
  - 600 MB/sec in ‘97
  - 700-800 MB/sec in ‘98
  - 1.6-2.4 GB/sec in ‘99 (Direct DRAM with 2-3 channels)
  - 3-4GB/sec in ‘01

The Rambus Channel
Design Standard Mindset

- The Channel Architecture is intended to be constant over multiple generations
- System Designers shouldn’t modify the Channel Architecture
- Improved compatibility and performance across multiple vendors’ memory controllers and DRAM

The Rambus Channel
Design and Implementation Discipline

- Rigid adherence to Rambus Channel dogma insures consistent and reliable high bandwidth
- Channel data width is intended to be held narrow regardless of memory population
- *Primary* Channels designed to support up to 32 RDRAMs or may be bridged to support 10 *Secondary* Channels (of 32 RDRAMs each)
- Bandwidth scaling
  - by use of multiple channels
  - by increasing the clock frequency

The Rambus Channel

The Center of Rambus-based Designs

- narrow data bus (8 or 9-bits of data) highly optimized for board-level platforms
- controlled impedance transmission line with predictable bus delays
- sophisticated synchronous clocking with minimal skew
- split-transaction packet protocol implements block transactions between masters and slaves

Rambus Channel
High-quality Transmission Lines

- Topology
  - master at one end
  - characteristic-trace-impedance terminators at the other end
  - slaves in between
- Implementation Discipline
  - dense/narrow bus with only 15 active signals
  - controlled impedance traces
  - short, dense packaging with minimized parasitics
  - matched, uniform loading
  - no discontinuities

Rambus Channel

Rambus Signaling Logic (RSL)

- Low voltage swings (600-800 mV)
  - reduced EMI, power, ground bounce
  - Logic 0 corresponds to V_{term} ~ 2.5V
  - Logic 1 corresponds to V_{OL} ~ 1.9V
- Differential sensing about bused Voltage Reference signal (V_{ref} approx. 2.2V)
  - provides common mode noise immunity

Rambus Channel
Skewless Data Clocking

- Clocks and data propagated in parallel down matched transmission lines
- ClkToMaster
  - from terminator side of channel
  - used to synchronize slave data sent to master
- ClkFromMaster
  - “loop back at Master” version of ClkToMaster
  - used to synchronize master data sent to slaves
- Data is transferred on both clock edges
- Each master or slave has two PLLs for clock extraction
- Master/slave internal clocks are twice the external clock

Rambus Channel

15 Active Signals, 28 total pins

- 13 Low-voltage-swing signals
  - BusData (8 or 9-bit data “byte”)
  - BusEnable
  - BusCtrl
  - ClkToMaster
  - ClkFromMaster
- SIn and SOut (daisy chained TTL device initialization signals
- V_{ref} (Voltage reference, which sets the logic threshold)
- Gnd, V_{dd} (power)
- GndA, $V_{dd}A$ (“Analog” power for PLLs)
- 2 isolation pins
- 1 reserved pin

The Rambus Channel
Logical Layer

- Packet protocol
  - Packets types include: Request, Acknowledge, Data
- Request Packet Format
  - 6 *intervals* x 10-bits per interval
  - start bit, 4-bit opcode, 36-bit address, 8-bit count
  - physical channel interface need not change with DRAM densities
- Transactions
  - Read/Write/Broadcast
  - Memory/Register Spaces
  - Multiple split-transactions outstanding
- 1-to-256-byte block transfers

Rambus Interface
Integral to Masters and Slaves

- Functions
  - Signaling conversion between the Rambus Channel and CMOS-cores
  - PLL-based synchronization of data to off-chip clocks
  - Generates/Decodes request packets (Masters/Slaves)
  - Implements acknowledge protocol, including multi-byte transfers
  - Couples addressed memory location from array sense amp latch to channel (Slaves)
- Electrical optimization
  - Current-drive (I-drive) transceivers
  - Optimized layout and packaging
    - pads, leads, traces are aligned and uniform in length
    - controlled impedance, minimal inductance
- ***Rambus ASIC Cell*** (RAC) available as module from Rambus

RDRAM (Rambus DRAM)

- Latest parts feature “concurrent RAS and CAS strobing”
  - internal interleaved bank organization, each with separate control
    - 2 banks in 16Mbit
    - 4 banks in 64Mbit
  - RAS and CAS for overlapped split-transactions to different banks can be concurrent
  - intended to permit hiding of page misses in systems that support split-transactions
- Large page-size compared to conventional DRAM
- 8-byte internal data bus, single byte external data bus organization
- Adds 4 additional core-power pins over Channel pins (32 total pins)

Other Rambus Architectural Features

- Read-only Registers
  - device type, size, manufacturer’s ID
- Programmable Control Registers
  - address mapping
  - power management
  - refresh
  - transaction timing
- Serial daisy-chain (SIn and SOut pins)
  - base memory address programmed during initialization
  - system refresh requests during power down

High Bandwidth in Small Capacity and Small Pinout Memory Systems

The Rambus Appeal

- Reduced need for additional memory access width
  - helps avoid the *Granularity* problem
- Reduced need for special memory architectures
  - e.g., SRAM caches, VRAM
- Reduced need for special technologies
  - e.g., MCMs
- Reduced costs from smaller packaging and routing
- Particularly well suited to video memory and UMA platforms

Complaints about Rambus
Sour Grapes?

- Appeal inversely proportional to Channel slave population
  - decreasing ratio of bandwidth-to-memory capacity
  - increased contention for single narrow bus
  - cumulative power dissipation of multiple PLLs per chip
- High signaling voltages relative to emerging sub-micron processes
- Patent royalty model viewed as overreaching
  - an up front licensing fee, plus royalties rumored at 2-5% of sales price of every device with a Rambus Interface (royalty incurred on both DRAM and core logic)
- Recent ties with Intel raises fears of undue Intel/Rambus influence over DRAM industry

Rambus Business Overview

- Located in Mountain View, CA
- Geoff Tate is President and CEO
- Founded in 1990 by Mike Farmwald and Mark Horowitz
- Production began in 4Q95
- licensees sold 10M units in ‘96 for $400M in revenue
- 30-40M units forecast for ‘97
- Many design wins
  - SGI Indigo, Nintendo 64, Chromatic Research Mpact multimedia processor, Microsoft Talisman, future Intel Core Logic parts
- Many RAM and Core Logic manufacturers are licensees
  - Hitachi, Hyundai, IBM, LG Semicon, LSI, NEC, Oki, Samsung, Toshiba

Rambus Patents

- Issued patents attempt to cover various attributes of Rambus Channel, Rambus Interface, and Rambus DRAM:
  - Method for Accessing and Transmitting Data To/From a Memory in Packets
  - Integrated Circuit I/O Using a High Performance Bus Interface
  - Apparatus for Synchronously Generating Clock Signals in a Data Processing System
  - High Speed Bus System
  - Electrical Current Source Circuitry for a Bus
- At least 5 patents have issued, totaling 113 claims, from the earliest application, filed in April of 1990

Direct DRAM

aka nDRAM (next DRAM), RDRAM II, Rambus 2

- Next generation Rambus Channel and Interface
- Requires new interface for core-logic and motherboards over original Rambus Interface
- Typical configuration to use multiple channels
  - 2, 9-bit, channels at 1.6 GB/sec
  - 3 channels for 2.4 GB/sec
- Improve the efficiency of the Rambus packet protocol
- Revamped signaling voltages?

Direct DRAM: *A Rambus/Intel Joint Development*

- Significant endorsement of Rambus technology and position by Intel
- Intended to supplant SDRAM at above 100MHz speeds
- Rambus will publish the specification
- Intel licensed for a Rambus-designed Direct DRAM Interface
- Targeted for 64Mbit, Christmas ‘99 Merced systems
- Expected to be adopted by all Rambus Licensees

Direct DRAM from Intel's Perspective

- Intel must be proactive in platform technologies
  - insure high growth in PC sales
  - integral to its overall business model
- In order to satisfy "an insatiable need for memory bandwidth," Intel began a major DRAM architectural evaluation in '95

Intel vs. the DRAM Vendors

- Vendors were not providing for the performance needs of future Intel-processor-based platforms
- Intel had core-logic problems from “incompatible” timings in 66-MHz SDRAMs
- Vendors were “encouraged” to contribute substantive engineering resources to Intel’s DRAM evaluation
- No timely vendor consensus for a SDRAM technology roadmap
- Vendors offered no viable alternative to using DIMM-based SDRAMs beyond 100-MHz
- Vendor proposals disparaged
  - design-by-committee efforts are moving too slow
  - will eventually need all of the features of the already proven Rambus

Direct DRAM's Impact

- Likely PC Industry Standard for 64Mbit and beyond
  - unless a viable open alternative is developed very soon
- Another Intel head start in platforms technology
  - infrastructure for '99 core logic already being established