Quick and Dirty List for Utilizing the Write-Back Cache on IBM 486DX2 Processors

Application Note

The following is a simple checklist of those items which must be properly set or examined to insure that the IBM 486DX2 processor is ready to execute its write-back cache mechanism:

- CR0 Register, Bit 29 (NW - Not Write-through), must be set to a logic '1' to operate in write-back mode.

- CR0 Register, Bit 30 (CD - Cache Disable), must be set to a logic '0' to insure that cache fills, in general, occur.

- CCR2 Register, Bit 1 (WBAK - Enable Write-Back Cache Interface Pins), must be set to a logic '1' to actually enable the I/O pins (INVAL, WM_RST, and HITM#) needed for the write-back caching mechanism.

- CCR2 Register, Bit 2 (LOCK_NW - Lock the NW bit), must be set to a logic '1' to insure that the value of the NW bit in the CR0 register cannot be changed.

- Check the Write-back cache pin interfaces (INVAL and HITM#) to the planar chipsets to insure proper electrical connections.

- CCR2 Register, Bit 4 (WT1 - Write-Through Region 1), must be set to a logic '0' to insure that **all** memory addresses (including the 640 kbyte to 1 Mbyte region) will be utilized as write-back. (Performance Enhancement ONLY)

- CCR1 Register, Bit 4 (NO_LOCK - Negate LOCK#), must be set to a logic '1' to insure that normally uncacheable read cycles (read cycles which are implemented with the LOCK# pin asserted and the KEN# pin asserted) are now forced to execute as cacheable cycles. (Performance Enhancement ONLY)

- CCR2 Register, Bit 6 (BWRT - Enable Burst Write Cycles), must be set to a logic '1' to insure that 16-byte burst write-back cycles occur. (Performance Enhancement ONLY)