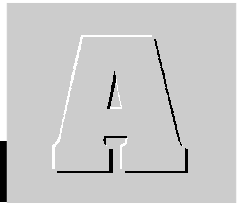

Ordering Information for Module Revision Level "B" Only

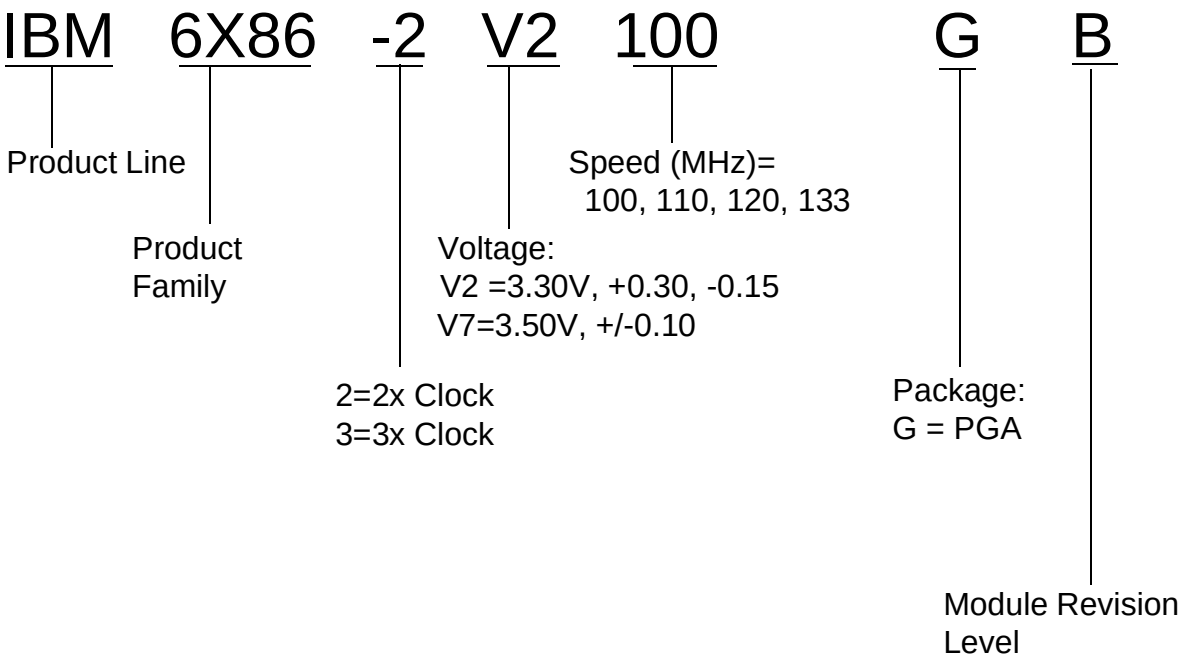

Table A-1. 6x86 Device to P-Rating Conversion

6x86 Frequency (MHz)		P-Rating
BUS	CORE	
50	100	P120+
55	110	P133+
60	120	P150+
66	133	P166+
75	150	P200+

Ordering Information for Module Revision Level "C" and Later

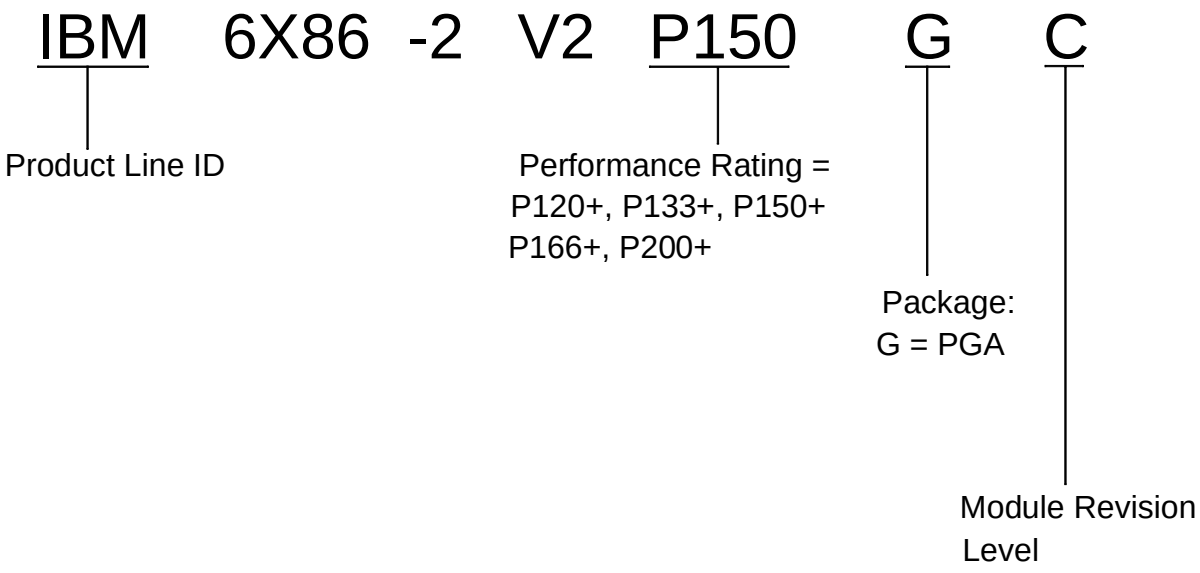

Table A-2. 6x86 Device to P-Rating Conversion

6x86 Frequency (MHz)		P-Rating
BUS	CORE	
50	100	P120+
55	110	P133+
60	120	P150+
66	133	P166+
75	150	P200+

For more information concerning the IBM 6x86 Microprocessor, please visit our website: *http://www.chips.ibm.com/products/x86/index.html* or call 1-800-IBM-3333.

INDEX

"1+4" Burst Read Cycle 3-35

A

AC Characteristics 4-5

Address Bus 3-9
Address Region Registers (ARRx) 2-31
Address Space 2-40
Architecture Overview 1-1

B

Back-Off Timing 3-49
Branch Control 1-11
Burst Cycle Address Sequence 3-34
Burst Write Cycles 3-37
Bus Arbitration 3-16
Bus Arbitration 3-46
Bus Cycle Definition 3-11
Bus Cycle Types 3-12
Bus Cycles, Non-pipelined 3-29
Bus Hold, Signal States During 3-17
Bus Interface 3-1
Bus Interface Unit 1-16
Bus State Definition 3-26

C

Cache Coherency Signals 3-18
Cache Control 3-14
Cache Control Timing 3-43
Cache Disable 2-34
Cache Inquiry Cycles 3-50
Cache Units 1-12
Caches, Memory 2-52
CCR0 Bit Definitions 2-25
CCR1 Bit Definitions 2-26
CCR2 Bit Definitions 2-27
CCR3 Bit Definitions 2-28
CCR4 Bit Definitions 2-29
CCR5 Bit Definitions 2-30
Clock Control 3-7
Clock Count for CPU Instructions 6-13
Clock Count for FPU Instructions 6-29
Configuration Control Registers 2-23
Control Registers 2-13

D

Data Bus 3-10
Data Bypassing 1-10
Data Forwarding 1-7
DC Characteristics 4-4
Debug Registers 2-37
Descriptors 2-16
Descriptor Table Registers and Descriptors 2-15
Device Identification Registers 2-36
DIRx 2-36

E

Electrical Specifications 4-1
Error Codes 2-62
EWBE# Timing 3-45
Exceptions 2-56
Exceptions in Real Mode 2-61

F

Flags Register 2-9
Floating Point Unit 1-15
FPU Error Interface 3-19
FPU Operations 2-75
Functional Blocks 1-1
Functional Timing 3-25

G

Gates and Protection 2-73

I

I/O Address Space 2-41
Initialization and Protected Mode 2-73
Initialization of the CPU 2-1
Instruction Fields, General 6-2
Instruction Line Cache 1-13
Instruction Pointer Register 2-9
Instruction Set Overview 2-3
Instruction Set Encodings and Summary
Instruction Set Summary 6-1
Instruction Set Tables Assumptions 6-12
Integer Unit 1-2
Interrupt Acknowledge Cycles 3-41
Interrupt and Exception Priorities 2-59
Interrupt Control 3-13
Interrupt Vectors 2-57
Interrupts and Exceptions 2-55

J

JTAG Interface 3-24

L

LBA# 2-35
Lines, within the Cache 2-53
Lock Prefix 2-3

M

Maximum Ratings, Absolute 4-2
Memory Addressing 2-43
Memory Addressing Methods 2-41
Memory Management Unit 1-14
MESI States, Unified Cache 2-52
Mode State Diagram 2-70

N

NC and Reserved Pins 4-1
Non-pipelined Bus Cycles 3-29

O

Offset Mechanism 2-42
Out-of-order Processing 1-4

P

Package, Mechanical Drawing 5-4
Paging Mechanisms (Detail) 2-45
Paging Mechanisms (Introduction) 1-14
Paging - Traditional Mechanism 2-45
Paging - Variable-Size Paging Mechanism 2-51
Pin Diagram, 296-Pin SPGA Package 5-1
Pin List, Sorted by Pin Number 5-2
Pin List, Sorted by Signal Name 5-3
Pipeline Stages 1-3
Pipelined Bus Cycles 3-38
Power and Ground Connections 4-1
Power Management Interface 3-22
Power Management Interface Timing 3-61
Privilege Level, Requested 2-8
Privilege Levels 2-71
Programming Interface 2-1
Protected Mode Address Calculation 2-44
Protection, Segment and Page 2-71
Pull-Up and Pull-Down Resistors 4-1

R

RAW Dependency Example 1-8
Recommended Operating Conditions 4-3
Region Control Registers (RCRx) 2-33
Register Renaming 1-4
Register Sets 2-4
Registers, Control 2-13
Registers, General Purpose 2-4
Registers, 6x86 Configuration 2-23
Registers, System Set 2-11
Requested Privilege Level 2-8
Reset Control 3-7
RESET Timing 3-25

S

Scatter/Gather Buffer Interface 3-19
Scatter/Gather Buffer Interface Timing 3-56
Sectors, Cache 2-53
Segment Registers 2-7
Selector Mechanism 2-44
Selectors 2-7
Shutdown and Halt 2-69
Signal Description Table 3-2
Signal Groupings 3-1
SMI# Interrupt Timing 3-42
System Management Mode (SMM) 2-63
SMM Instructions 2-67
SMM Memory Space 2-68
SMM Memory Space Header 2-65
SMM Operation 2-64
Stop Grant (Special Bus Cycle) 3-12
Stop Grant and SUSP# 3-22
Speculative Execution 1-12
Suspend Mode, HALT Initiated 3-62
Suspend Mode, Signal States During 3-23
System Management Mode 2-63

T

Task Register 2-20
Test Registers 2-39
Testing of the Unified Cache 2-53
Thermal Characteristics 5-6
Timing, Functional 3-25
Translation Lookaside Buffer 2-45
Translation Lookaside Buffer Testing 2-47

U

Unified Cache 1-12
Unified Cache Testing 2-53

V

Variable-Size Paging Mechanism 1-14
Variable-Size Paging Mechanism 2-51
Virtual 8086 Mode 2-74

W

WAR Dependency Example 1-5
WAW Dependency Example 1-6
Weak Locking 2-34
Weak Write Ordering 2-34
Write Gathering 2-35
Write Through 2-35