Board Analysis and Practices for High Speed Motherboard Design

Overview

The rapid increase in microprocessor clock speeds over the past years is continually challenging motherboard designers with meeting timing margins, clocking and signal quality. With the latest introduction of IBM's 6x86MX™ Microprocessor containing an 83 MHz external host bus, the motherboard designer is faced with even tighter timing constraints.

While the industry is currently positioned at 66 and 75 MHz buses, companies like IBM are moving toward increased host bus speeds to complement their processor's architectural performance features. In response, board analysis is becoming focused on assuring a reliable product while providing constructs aiding in the reduction of development time.

This application note provides the system designer with information to be used in conjunction with good engineering practices for analysis of motherboard design. After completing the recommended board analysis, further detailed analysis using I/O buffer models from associated semiconductor manufacturers is strongly recommended.

Analysis Outline

The following outline is provided to guide the motherboard designer in developing a high speed motherboard design. The methodology outlined is based on current design recommendations and motherboard experience. All formulas and recommendations are provided to give insight, and under no means dictate a hard and fixed methodology.

- Timing margins
- Clocking
- Physical design
  - Board layout
  - Routing
- Board validation

Timing Margins

Timing analysis provides a baseline to the designer on the amount of cycle time margin for a given clock frequency. This margin can then be used to tailor I/O interfaces to assure compliance with device manufacturer's timing specifications. Using the following formula, the amount of margin available for a given device's interface can be calculated.

$$T_{Margin} = T_{CT} - T_{DV} - T_{SU} - T_{Flight}$$

T_{Margin} Formula Definitions

Variable	Definition
T_{Margin}	Margin Time
T_{CT}	Cycle Time
T_{DV}	Data Valid
T_{SU}	Setup Time
T_{Flight}	Flight Time

To ensure proper analysis of the design, the interface topology can be broken down into subsystems and then divided into I/O categories. This practice allows for an early detection of timing problems and a complete analysis. See Appendix A for a detailed analysis of a CPU-to-core chipset.

Cycle Time (T_{CT})

Cycle time is defined as the amount of time per given clock period.

$$T_{CT} = 1 / \text{Clock Frequency}$$

$$12ns = 1 / 83\ MHz$$

Cycle Times

Clock Frequency (MHz)	Cycle Time (ns)
8 ISA Bus	125
33 PCI Bus	30
60 CPU Host	16.6
66 CPU Host	15
75 CPU Host	13
83 CPU Host	12

Data Valid (T_{DV})

Data valid is the amount of time it takes a signal to travel from the internal circuitry to the I/O pin of the device within a given clock cycle. This value is specified per a given capacitive load. The designer is required to determine the relative capacitive loading for each signal net. Sources of capacitive loading include the following:

- Other devices attached to the trace
- Connectors
- Board/trace
- Sockets

In the case where the design point does not meet or exceeds the capacitive rating, the designer needs to obtain a derating formula or curve for the device. From the following example formula, a prorated value can be determined.

$$\text{Derating} = 0.016\text{ns / pF} * C_{Delta}$$

where $C_{Delta} = C_{actual} - C_{rated}$

If assuming a C_{rated} of 35pF with a C_{actual} of 50pF, the result is an increase of about 0.24ns to Data Valid.

Setup Time (T_{SU})

Setup time is the time required by the receiving device for the data to be stable at its input pin before the next clock cycle.

Note: At this phase of the timing analysis, the designer should not factor in any skewing due to ringback and/or undershoot. These factors will be assessed after early placement and routing.

Flight Time (T_{Flight})

Flight time is composed of multiple board and component variables giving the designer some flexibility in tuning the overall timing margin.

$$T_{Flight} = T_{ClkSkw} + T_{ClkJitter} + T_{BrdFlight}$$

where T_{ClkSkw} is defined as the clock skew time between outputs for a given clock generator. This information is provided on manufacturer's data sheets, for example, a clock skew range from ±150 to 500ps.

where $T_{ClkJitter}$ is defined as the amount of clock jitter, or variance, for a given clock per clock cycle. For example, the IBM 6x86MX Microprocessor requires a clock stability of ±250ps.

where $T_{BrdFlight}$ is defined as board flight time, or the time required for a signal to travel from the driver, and then be seen by the receiver. Flight time determination involves:

- Motherboard material selection
- Propagation time calculation
- Analysis mode of trace for RC time constant or transmission line

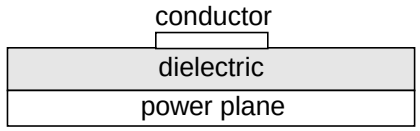
By using the following formulas with a dielectric selection, the propagation time for the signal trace can be calculated. These formulas provide a relatively accurate analysis for general propagation time. For a more detailed analysis, refer to a reference book on transmission line analysis and/or motherboard design.

Microstrip:

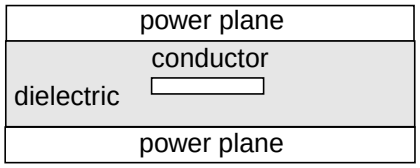
$T_{Travel} = 0.004 * \text{SQRoot}(0.45E_r + 0.67)$ns per mm

Stripline:

$T_{Travel} = 0.004 * SQRoot(E_r) ns\ per\ mm$



Microstrip



Stripline

Dielectric Constants (E_r)

Material	Dielectric Constant (E_r)
TLE	2.95
R4003	3.38
Cyanate Ester (S-Glass)	3.5
FR-4 Getek Epoxy/PPO	3.9
BT/Epoxy	4
Polyimide	4.3
FR-4	4.5

After calculating T_{Travel}, the determination of the signal trace analysis can be done using:

$$T_L < T_R / (2 * T_{Travel})$$

where T_L = trace length, and T_R = rise time

If the inequality is true, the signal trace can be treated as an RC time constant. Otherwise, transmission line analysis is required.

Transmission line analysis provides a means to develop the trace definition for high frequency signals containing the fast rise and fall times. It is recommended for the designer to use simulation software to model their distributed circuit trace. The analysis will provide information on signal quality aspects such as overshoot, undershoot, ringback, reflection, and driver/receiver impedance mismatch.

Termination

To ensure signal quality, the use of termination on transmission lines is recommended and needs to be balanced with available layout real estate. Four types of termination are used throughout various motherboard designs.

Series

Series termination is commonly used to match the output impedance of drivers to the characteristic impedance of the signal trace. The impedance matching results in less reflective waves being generated for a given trace. While the overall power consumption is low with series termination, the method does increase rise and fall times.

Note: The voltage drop across the series resistor may cause problems with noise margins associated with V_{IH} and V_{IL}.

Pull-up/Pull-down

While mainly used to connect a TTL-level output to a CMOS-level input, some designers have used this form of termination to reduce trace ringing. One major drawback of this termination network is the DC power consumption.

RC

RC termination provides a means of removing the noise glitches from a signal trace without the introduction of a DC current source. The noise removal is achieved by selecting Rs and Cs that provide a frequency filter, but in turn do not attenuate the signal rise and fall times.

Diode Clamping

This method uses two Schottky diodes tied to a Vcc and ground network to prevent overshoot and undershoot. The use of this termination provides a means that does not impact the overall impedance matching of the trace.

Clocking

General

IBM's 6x86MX CPU with an 83 MHz external bus requires the designer to contend with tighter constraints on clock distribution and skewing. With the fast rise and fall times associated with the clock edges, transmission line analysis is recommended. This analysis will aid in providing for a precise clock layout topology meeting the specified clock requirements.

Clocking Issues

By addressing the fast rise/fall times and analyzing trace lengths greater than TR / (2 * T_{Travel}), issues like overshoot, undershoot, and ringback can be minimized. Oversight of these issues will result in distorted waveforms producing false triggering and a non-synchronous design point.

To minimize these effects, each clock net is recommended to have a form of termination. As described in the Timing Margins section, the designer has four choices: series, pull-up/pull-down, RC, and diode clamping.

With series termination providing a low power consumption method and aiding in reducing the reflection off the driver, this is a common choice for clock nets. When analyzing the effects of termination, the designer needs to factor in both the output rise and fall impedance values.

With the increase in frequency, the designer is faced with less margin for clock skew in a synchronous design. This requirement, while typically in the range of ± 250ps, is becoming a critical factor in the overall timing budget.

To minimize skew between devices, the choice of clock generator can control whether the clock network is balanced or unbalanced. For balanced, each trace length is matched to all others of the same frequency. The designer is recommended to place the clock generator as close as possible to the CPU/Core chipset. In cases where a connector is inserted in the clock network, Spice modeling and transmission analysis is recommended.

For an unbalanced clock network, the designer will be required to tune the network by varying the trace length and possibly the form of termination. Any load imbalance will increase the manufacturer's stated skew. When possible, the design point should focus on a balanced network topology with no connectors inserted into any of the high frequency/fast rise edge rate clock nets.

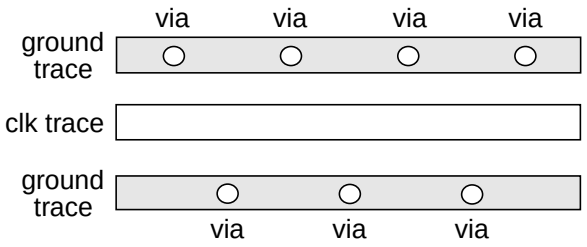
6x86MX Clock Specifications

Description	Minimum	Maximum	Unit
Frequency		83	MHz
Period	12		ns
Stability		± 250	ps
Rise Time	0.15	1.5	ns
Fall Time	0.15	1.5	ns
High Time	4		ns
Low Time	4		ns

Clock Routing

The following are recommended practices:

- Route all clock nets first before embedding signal traces.
- Route all clock lines in the internal signal planes of the motherboard.
- Place all series terminations as close as possible to the associated clock generator output pin.
- When large amounts of added trace are required to match associated nets, break up the trace jogs into smaller groups.
- Signal keep-out defined on surface layer under all clock generators and associated crystals.
- Ground-shield all clock lines as shown:



Note: Vias attached to ground.

Physical Design

Board Layout

With a wide range of motherboard profiles, board real estate can vary from one extreme to the other. In either case, when designing high frequency layouts, location and grouping of core functions is key. By grouping each core, the designer can control “hot spots” for the routing. These hot spots define high density routing within the board layers. Ways to relieve hot spots are:

- Growing the numbers of layers
- Decreasing trace width
- Swapping vertical and horizontal trace layers
- Regrouping of core functions
- Device packaging

Routing

Depending on design schedule and complexity, the designer has a choice of either hand routing or autorouting. Either method requires the designer to be proactive with the physical designer to achieve a quality result.

To help in the communication, designers can provide a physical design file containing key attributes about the layout topology. See Appendix B for more information. Appendix C contains an example setup file for an autorouter. In addition, attention needs to be applied to understanding what tradeoffs will occur when transitioning between the trace analysis and routing. Examples are given in the following table.

Routing Analysis

Analysis	Routing
Daisy chain nets with no stubs	Depending on trace density, choosing no stubs will cause increased wiring lengths and create additional “hot spots.” Set stub length to 300-500 mils.
Termination required on large buses	Depending on choice of termination and bus size, the real estate for the termination can be very large, for example, two SMT 805 package size resistors require about 1/4 square inch. To reduce the area, impedance match the board trace to the driver and select a core chipset that matches the impedance of the overall board topology.
Use of decoupling when traces cross split power planes.	Depending on number of additional capacitors, real estate problems can occur. Add an extra power plane or redefine the voltage cross section.

Board Validation

Board validation and back annotation provide the designer with a means to correlate lab results with analysis. While often overlooked, this phase of the analysis is key to developing a more accurate analysis model and formulas.

Appendix A

CPU-to-Core Chipset Analysis at 83 MHz

Clock frequency is 83 MHz; sample core chipset and clock generator. Table data shown prior to derating adjustment to core chipset.

Formulas

Cycle Time:

T_{CT} = 1 / Clock Frequency

Timing Margin:

$T_{Margin} = T_{CT} - T_{Flight} - T_{DV} - T_{SU} - T_{ClkSkw} - T_{ClkJitter}$

Flight Time:

T_{Flight} = Microstrip analysis

Input (Point-to-Point)

Signal Name	Motherboard					Chipset		CPU	
	Timing Margin (ns)	Clock Skew (±ns)	Clock Jitter (±ns)	Trace Length (in)	Flight Time (ns)	Data Valid (ns)	CL (pF)	Setup Time (ns)	CL (pF)
$\overline{A20M}$	1.4	0.250	0.250	10	1.7	5.5		3.0	50
AHOLD	2.9	0.250	0.250	10	1.7	3.5	35.0	3.5	50
$\overline{BOFF}$	2.9	0.250	0.250	10	1.7	3.5	35.0	3.5	50
$\overline{BRDYC}$	2.9	0.250	0.250	10	1.7	4.0		3.0	50
$\overline{BRDY}$	2.9	0.250	0.250	10	1.7	4.0	35.0	3.0	50
$\overline{EADS}$	2.4	0.250	0.250	10	1.7	4.5	35.0	3.0	50
IGNNE	2.7	0.250	0.250	10	1.7	5.5		1.7	50
INTR	2.2	0.250	0.250	10	1.7	6.0		1.7	50
INV	4.7	0.250	0.250	10	1.7	3.5		1.7	50
$\overline{KEN}$	3.4	0.250	0.250	10	1.7	3.5	35.0	3.0	50
$\overline{NA}$	4.7	0.250	0.250	10	1.7	3.5	35.0	1.7	50
NMI	3.2	0.250	0.250	10	1.7	5.0		1.7	50
$\overline{SMI}$	2.2	0.250	0.250	10	1.7	6.0	35.0	1.7	50
$\overline{SUSP}$	3.2	0.250	0.250	10	1.7	5.0		1.7	50
WM_RST	2.2	0.250	0.250	10	1.7	6.0		1.7	50

Output (Point-to-Point)

Signal Name	Motherboard					Chipset		CPU	
	Timing Margin (ns)	Clock Skew (±ns)	Clock Jitter (±ns)	Trace Length (in)	Flight Time (ns)	Setup Time (ns)	CL (pF)	Data Valid (ns)	CL (pF)
$\overline{\text{CACHE}}$	2.9	0.250	0.250	10	1.7	3.0		4.0	50
$\overline{\text{D/C}}$	2.9	0.250	0.250	10	1.7	3.0		4.0	50
$\overline{\text{HITM}}$ [note]	0.9	0.250	0.250	10	1.7	5.0		4.0	50
$\overline{\text{LOCK}}$	2.9	0.250	0.250	10	1.7	3.0		4.0	50
$\overline{\text{M/IO}}$	2.9	0.250	0.250	10	1.7	3.0		4.0	50
$\overline{\text{SMIACT}}$	2.9	0.250	0.250	10	1.7	3.0		4.0	50
$\overline{\text{W/R}}$	2.9	0.250	0.250	10	1.7	3.0		4.0	50

note: $\overline{\text{HITM}}$ for some chipsets is a 2-cycle path

Output (Multidrop)

Signal Name	Motherboard					Chipset		CPU	
	Timing Margin (ns)	Clock Skew (±ns)	Clock Jitter (±ns)	Trace Length (in)	Flight Time (ns)	Setup Time (ns)	CL (pF)	Data Valid (ns)	CL (pF)
$\overline{\text{ADS}}$	2.5	0.250	0.250	9	1.5	3.5		4.0	50

Bi-directional (CPU-to-Chipset, Point-to-Point)

Signal Name	Motherboard					Chipset		CPU	
	Timing Margin (ns)	Clock Skew (±ns)	Clock Jitter (±ns)	Trace Length (in)	Flight Time (ns)	Setup Time (ns)	CL (pF)	Data Valid (ns)	CL (pF)
A31-A19	-7.0	0.250	0.250	9	1.5	13.0		4.0	50

note: Address bus for some chipsets is a 2-cycle path

Bi-directional (Chipset-to-CPU, Point-to-Point)

Signal Name	Motherboard					Chipset		CPU	
	Timing Margin (ns)	Clock Skew (±ns)	Clock Jitter (±ns)	Trace Length (in)	Flight Time (ns)	Data Valid (ns)	CL (pF)	Setup Time (ns)	CL (pF)
A31-A19	1.0	0.250	0.250	9	1.5	6.0		3.0	50

Bi-directional (CPU-to-Chipset, Multidrop)

Signal Name	Motherboard					Chipset		CPU	
	Timing Margin (ns)	Clock Skew (±ns)	Clock Jitter (±ns)	Trace Length (in)	Flight Time (ns)	Setup Time (ns)	CL (pF)	Data Valid (ns)	CL (pF)
A18-A3 [note]	-7.0	0.250	0.250	9	1.5	13.0		4.0	50
D63-D0	2.9	0.250	0.250	10	1.7	2.0		5.0	50
$\overline{BE7}$-$\overline{BE0}$	2.7	0.250	0.250	11	1.8	3.0		4.0	50
note: Address bus for some chipsets is a 2-cycle path									

Bi-directional (Chipset-to-CPU, Multidrop)

Signal Name	Motherboard					Chipset		CPU	
	Timing Margin (ns)	Clock Skew (±ns)	Clock Jitter (±ns)	Trace Length (in)	Flight Time (ns)	Data Valid (ns)	CL (pF)	Setup Time (ns)	CL (pF)
A18-A3	1.0	0.250	0.250	9	1.5	6.0		3.0	50
D63-D0	3.7	0.250	0.250	10	1.7	4.5		1.7	50

Appendix B

Physical Design Data File

Card Characteristics

Card thickness: 0.062", ± 0.008

Power plane: 2 oz/sq. ft., copper

Signal planes: 0.5 oz/sq. ft., copper

Board Stackup

- Signal spacing, 6 mil traces, 6 mil spaces
- 50 ohm stackup for all signal layers
- Smallest via size should be 0.012 mil
- Layers, top to bottom:
  1. Signal
  2. Power, ground
  3. Signal
  4. Signal
  5. Power, +3.3V, Vcc I/O, Vcc Core
  6. Signal

Placement Information

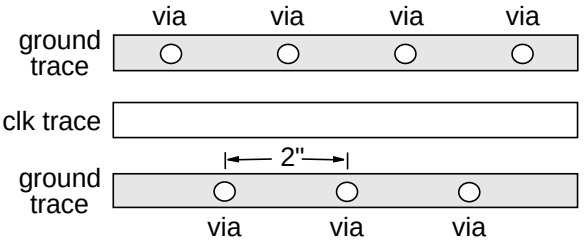
- Connectors cannot be moved.
- Approximate placement of components as per mechanical recommendation.
- Discrete components such as Rs and Cs may be moved for better wiring, but should stay near the component and pins by which they were placed as written in the schematic pages.
- Put the decoupling caps near each Vcc as mentioned in schematics.
- Tag ram shall be placed on backside of board behind CPU.
- Wiring shall be 6" or less for every net, and should have balanced propagation time for similar nets (address bus, data bus, etc.). See Wiring Groups, next, for details.
- If any I/O signals cross a power plane boundary (power plane is split into I/O power and Core power), capacitors will be necessary to connect the two power places together in the frequency domain. These capacitors are included in the schematic.
- A Core power sense net is included between an actual Core power pin on the 6x86MX processor and the on-board power supply. This trace should be routed on a single layer with no vias.

Wiring Groups

- No 90 degree angles or T junctions. Any stubs shall be <= 0.3 inches in length.
- All clock signals should have ground surround shields. Clocks should be wired first, on internal signal planes only.
- Wire targets for characteristic impedance shall be 50 ohms.
- Power and ground traces should be as short as possible. Use either 12 or 16 mil breakout traces.
- Vias should be placed on a 25 mil grid. Use smaller grids only in cases of emergency.

Clock Wiring

- All clock traces need to be shielded using a ground via every 2 inches on a side, with each side offset by 1 inch on via locations.



Note: Vias attached to ground.

- To minimize clock skew, trace lengths associated with a particular clock group (33 MHz, 83 MHz, etc.) must be matched to within 1/2".

- Clock names:
  - CPU Clock
  - SRAM Clock #1
  - SRAM Clock #2

Special Wiring Considerations

Ensure that routed nets are scheduled correctly to minimize trace length. Wire these nets in the following order:

1. Daisy-chained signals group:
   - Address bus
   - Data bus
   - Byte enable (BE)
   - Cache output enable
   - Cache burst address advance
   - Address strobe
   - Cache address strobe
   - Cache byte write enable
   - Global write
   - Burst mode
2. Point-to-point connections group
   - Tag address
   - Next address
   - Burst ready
   - Back off
   - Address hold
   - Hold request
   - Cache hit modified data
   - Cache enable

Appendix C

Router Control Data File

```
forget class one

forget class two

forget class three

forget class four

forget class five

grid via 50

grid wire 1

rule pcb (tjunction term_only)

cost off_grid forbidden

define (class one -HEADS -HBRDY -HBE0 -HBE1 -HBE2 -HBE3 -HBE4 -HBE5 -HBE6 -HBE7 -
HKEN -HM/IO -HCACHE MA1 MA2 MA3 MA4 MA5 MA6 MA7 MA8 MA9 MA10 MA11 MD0 MD1 MD2 MD3
MD4 MD5 MD6 MD7 MD8 MD9 MD10 MD11 MD12 MD13 MD14 MD15 MD16 MD17 MD18 MD19 MD20
MD21 MD22 MD23 MD24 MD25 MD26 MD27 MD28 MD29 MD30 MD31 MD32 MD33 MD34 MD35 MD36
MD37 MD38 MD39 MD40 MD41 MD42 MD43 MD44 MD45 MD46 MD47 MD48 MD49 MD50 MD51 MD52
MD53 MD54 MD55 MD56 MD57 MD58 MD59 MD60 MD61 MD62 MD63 HD0 HD1 HD2 HD3 HD4  HD5
HD6 HD7 HD8 HD9 HD10 HD11 HD12 HD13 HD14 HD15 HD16 HD17 HD18 HD19 HD20 HD21 HD22
HD23 HD24 HD25 HD26 HD27 HD28 HD29 HD30 HD31 HD32 HD33 HD34 HD35 HD36 HD37 HD38
HD39 HD40 HD41 HD42 HD43 HD44 HD45 HD46 HD47 HD48 HD49 HD50 HD51 HD52 HD53 HD54
HD55 HD56 HD57 HD58 HD59 HD60 HD61 HD62 HD63 HA3 HA4 HA5 HA6 HA7 HA8 HA9 HA10
HA11 HA12 HA13 HA14 HA15 HA16 HA17 HA18 HA19 HA20 HA21 HA22 HA23 HA24 HA25 HA26
HA27 HA28 HA29 HA30 HA31)

define (class two PCI_AD0 PCI_AD1 PCI_AD2 PCI_AD3 PCI_AD4 PCI_AD5 PCI_AD6 PCI_AD7
PCI_AD8 PCI_AD9 PCI_AD10 PCI_AD11 PCI_AD12 PCI_AD13 PCI_AD14 PCI_AD15 PCI_AD16
PCI_AD17 PCI_AD18 PCI_AD19 PCI_AD20 PCI_AD21 PCI_AD22 PCI_AD23 PCI_AD24 PCI_AD25
PCI_AD26 PCI_AD27 PCI_AD28 PCI_AD29 PCI_AD30 PCI_AD31 PCI_PAR -PCI_RESET -
PCI_C/BE0 -PCI_C/BE1 -PCI_C/BE2 -PCI_C/BE3 -PCI_GNT0 -PCI_GNT1 -PCI_GNT2 -
PCI_GNT3 -PCI_REQ0 -PCI_REQ1 -PCI_REQ2 -PCI_REQ3 -PCI_FRAME -PCI_TRDY -PCI_IRDY
-PCI_STOP -PCI_DEVSEL -PCI_LOCK -PCI_SERR -PCI_PERR -INTA -INTB -INTC -INTD)

define (class three LA20 LA21 LA22 LA23 -IOR -IOW -MEMR -MEMW -SMEMR -SMEMW
IOCHRDY -IOCS16 -MEMCS16 -REFRESH RSTISA)

define (class four XD0 XD1 XD2 XD3 XD4 XD5 XD6 XD7 -ROMCS -SBHE SA0 SA1 SA2 SA3
SA4 SA5 SA6 SA7 SA8 SA9 SA10 SA11 SA12 SA13 SA14 SA15 SA16 SA17 SA18 SA19 SD0 SD1
SD2 SD3 SD4 SD5 SD6 SD7 SD8 SD9 SD10 SD11 SD12 SD13 SD14 SD15)

define (class five -CS0 -CS1 IDEA2 IDEA1 IDEA0 -IDEIOR1 -IDEIOR0 -IDEIOW1 -
IDEIOW0 -IDECHRDY -IDERST IDE_D0 IDE_D1 IDE_D2 IDE_D3 IDE_D4 IDE_D5 IDE_D6 IDE_D7
IDE_D8 IDE_D9 IDE_D10 IDE_D11 IDE_D12 IDE_D13 IDE_D14 IDE_D15 DRQX DRQY -DACKX -
DACKY)
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