Intel386™ CX/SXSA MICROPROCESSOR SPECIFICATION UPDATE

Release Date: January, 1997
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The Intel386™ CX/SXSA microprocessor may contain design defects or errors known as errata. Characterized errata that may cause the Intel386 CX/SXSA microprocessor's behavior to deviate from published specifications are documented in this specification update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 7641
Mt. Prospect IL 60056-7641

or call in North America 1-800-879-4683, Europe 44-0-1793-431-155,
France 44-0-1793-421-777, Germany 44-0-1793-421-333, other countries 708-296-9333

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REVISION HISTORY

Rev. Date	Version	Description
12/23/96	002	**Specification Changes** • IDIV instruction interrupt0 due to overflow
07/01/96	001	This is the new Specification Update document. It contains all identified errata published prior to this date.
04/10/95	1.00	**Device Package Mark Changes:** • Documents change indicator on package mark to reflect the device stepping Specification Changes: • Modified AC timing parameters in datasheet

PREFACE

As of July, 1996, Intel's Semiconductor Products Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
Intel386™ SXSA Embedded Microprocessor datasheet	272419-003
Intel386™ CXSA Embedded Microprocessor datasheet	272418-002
Intel386™ CXSB Embedded Microprocessor datasheet	272552-003
1996 Embedded Microprocessors Handbook	272396

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Intel386™ CX/SXSA processor product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

▌	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	#	#	#			
						None for this revision of this specification update.

Specification Changes

No.	Steppings		Page	Status	SPECIFICATION CHANGES
	A	B			
1	X	X	9	Doc	Changes to Intel386™ CX/SXSA Microprocessor AC Timing Specifications
2	X	X	9	Doc	IDIV Instruction Interrupt0 Due To Overflow

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	#	#	#			
						None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
				None for this revision of this specification update.

IDENTIFICATION INFORMATION

Markings

Intel386 CX/SXSA processors may be identified electrically according to device type and stepping. Refer to the data sheet for instructions on how to obtain the identifier number.

The *change indicator* is used to relate information found here and in other documents, like data sheets, to a specific device. The A-2 stepping version of the Intel386 CX and SXSA processor has the change indicator marked ‘A’. The B-stepping version of the Intel386 CX/SXSA processor is designated with a change indicator of ‘B’. Please note that the change indicator does not necessarily directly correspond to the stepping. Below is an illustration indicating where the change indicator marking is located on the package marking.

ERRATA

None for this revision of this specification update.

SPECIFICATION CHANGES

1. Changes to Intel386™ CX/SXSA Microprocessor AC Timing Specifications

The following AC timing characteristics are changes to the timingss published in the *Intel386™ CXSA/CXSB Embedded Microprocessor* and *Intel386™ SXSA Embedded Microprocessor* datasheets:

	Datasheet		A-2 Stepping		B Stepping	
	25 MHz	33, 40 MHz	25 MHz	33, 40 MHz	25 MHz	33, 40 MHz
T6 (min)	4	4	4	3	3	3
T12 (min)	7	7	4	4	7	7
T24 (min)	3	2	3	3	3	2

2. IDIV Instruction Interrupt0 Due To Overflow

ISSUE: The IDIV instruction operands need to be sign-extended to avoid incurring an overflow condition (interrupt0 exception).

An extremely limited subset of IDIV calculations may not properly generate an overflow interrupt0 exception subsequent to the actual occurrence of an overflow calculation. This inhibited interrupt0 exception condition results in an incorrect IDIV quotient calculation. The IDIV instruction does not incur the overflow condition when sign-extension is conducted before the operation. Direct assembly language programming should also perform sign-extension prior to executing IDIV to preclude the occurrence of the overflow condition (sign-extension of the divisor is used to prevent the overflow condition, sign-extension of the dividend is used to satisfy the IDIV instruction format). The Intel386 processor instruction set incorporates several commands to facilitate sign-extension. The CBW, CWD(CWDE), and CDQ instructions are often utilized to automatically sign-extend byte, word, and double-word data.

Fortran and C require that arithmetic operations be performed on operands of equal length; some compilers may already either extend the shorter operand or extend both operands to a common larger size. To accommodate both positive and negative numbers, these compilers typically establish this equal length by performing sign-extension.

SPECIFICATION CLARIFICATIONS

None for this revision of this specification update.

DOCUMENTATION CHANGES

None for this revision of this specification update.