PRELIMINARY

EMBEDDED ULTRA-LOW POWER Intel486™ SX PROCESSOR

SmartDie™ Product Specification

- **Ultra-Low Power Member of the Intel486™ Processor Family**
  - **— 32-Bit RISC Technology Core**
  - **— 8-Kbyte Write-Through Cache**
  - **— Four Internal Write Buffers**
  - **— Burst Bus Cycles**
  - **— Dynamic Bus Sizing for 8- and 16-bit Data Bus Devices**
  - **— Intel System Management Mode (SMM)**
  - **— Boundary Scan (JTAG)**
- **32-Bit External Data Bus**
- **Separate Voltage Supply for Core Circuitry**
- **Fast Core-Clock Restart**
- **Auto Clock Freeze**
- **Ideal for Embedded Battery-Operated and Hand-Held Applications**
- **Intel SmartDie™ Product**
  - **— Full AC/DC Testing at Die Level**
  - **— 0°C to +90°C (Junction) Temperature Range**

NOTICE: This document contains preliminary information on new products in production. It is valid for the devices indicated in "DEVICE NOMENCLATURE" on page 12. This specification is subject to change without notice. Verify with your local Intel sales office that you have the latest product specification before finalizing a design.

REFERENCE INFORMATION: The information in this document is provided as a supplement to the standard package datasheet on a specific product. Please reference the standard package datasheet (order number 272731) for additional product information and specifications not found in this document.

*Other brands and names are the property of their respective owners.

March 1996 **Order Number: 272820-001**

EMBEDDED ULTRA-LOW POWER Intel486™ SX PROCESSOR

SmartDie™ Product Specification

1.0 DIE SPECIFICATIONS

The die photo below and the plot on page 2 indicate the orientation of the die in the GEL-PAK* (shipping container). Die are aligned as shown relative to a 45° notch which is in one corner of the GEL-PAK. An Intel internal manufacturing name “Hummingbird” appears on the die. Table 1 describes the bond pad number and pad center data for each signal.

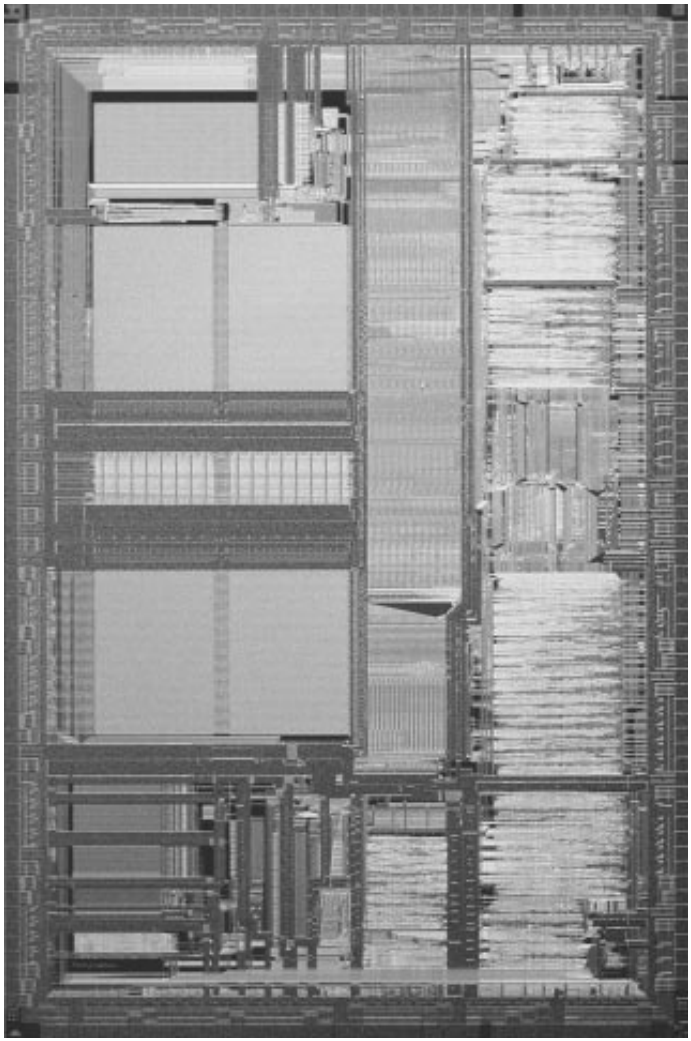


Figure 1. Embedded Ultra-Low Power Intel486™ SX Processor Die Photo

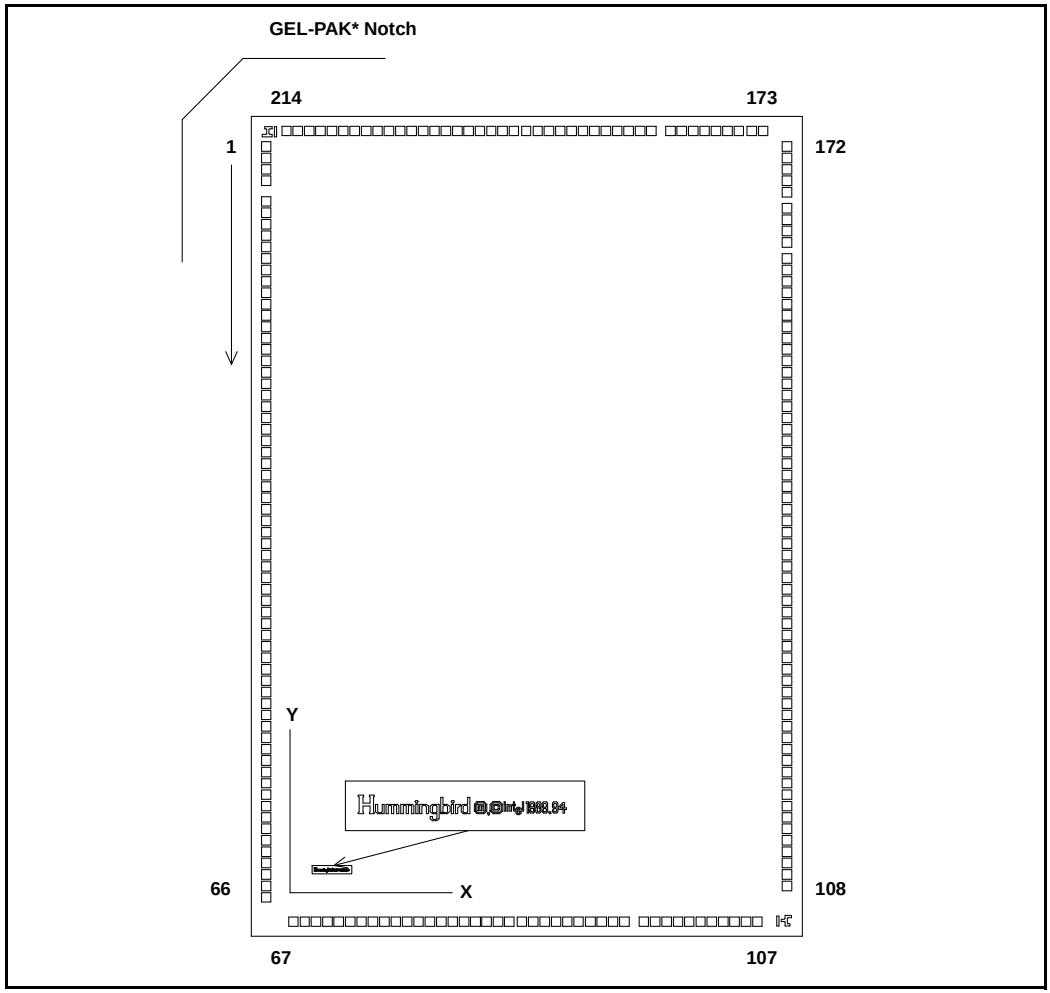


Figure 2. Embedded Ultra-Low Power Intel486™ SX Processor Die/Bond Pad Layout

Table 1. Embedded Ultra-Low Power Intel486™ SX Processor Bond Pad Center Data (Sheet 1 of 7)

PAD#	SIGNAL[2,3,4,5]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
001	V_{CCP}	-128.5	186.7	-3263	4742
002	V_{SS}	-128.5	181.1	-3263	4600
003	A21	-128.5	175.5	-3263	4457
004	A22	-128.5	169.9	-3263	4315
005	A23	-128.5	159.8	-3263	4058
006	A24	-128.5	154.2	-3263	3916
007	V_{CCP}	-128.5	148.6	-3263	3773
008	V_{SS}	-128.5	142.9	-3263	3631
009	A25	-128.5	137.3	-3263	3488
010	A26	-128.5	131.7	-3263	3346
011	A27	-128.5	126.1	-3263	3203
012	A28	-128.5	120.5	-3263	3061
013	V_{CCP}	-128.5	114.9	-3263	2918
014	V_{SS}	-128.5	109.3	-3263	2776
015	A29	-128.5	103.7	-3263	2633
016	A30	-128.5	98.1	-3263	2491
017	A31	-128.5	92.5	-3263	2348
018	N.C.	-128.5	86.8	-3263	2206
019	N.C.	-128.5	81.2	-3263	2063
020	D0	-128.5	75.6	-3263	1921
021	D1	-128.5	70.0	-3263	1778
022	D2	-128.5	64.4	-3263	1636
023	D3	-128.5	58.8	-3263	1493
024	D4	-128.5	53.2	-3263	1351
025	V_{CC}	-128.5	47.6	-3263	1208
026	V_{SS}	-128.5	42.0	-3263	1066
027	V_{CC}	-128.5	36.4	-3263	923
028	V_{SS}	-128.5	30.7	-3263	781
029	V_{CC}	-128.5	25.1	-3263	638
030	V_{SS}	-128.5	19.5	-3263	496
031	V_{SS}	-128.5	13.9	-3263	353
032	V_{CC}	-128.5	8.3	-3263	211
033	V_{SS}	-128.5	2.7	-3263	68

Table 1. Embedded Ultra-Low Power Intel486™ SX Processor Bond Pad Center Data (Sheet 2 of 7)

PAD#	SIGNAL[2,3,4,5]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
034	V_{CC}	-128.5	-2.9	-3263	-74
035	V_{SS}	-128.5	-8.5	-3263	-217
036	V_{CC}	-128.5	-14.1	-3263	-359
037	V_{CCP}	-128.5	-19.7	-3263	-502
038	V_{SS}	-128.5	-25.4	-3263	-644
039	D5	-128.5	-31.0	-3263	-787
040	D6	-128.5	-36.6	-3263	-929
041	V_{CCP}	-128.5	-42.2	-3263	-1072
042	V_{SS}	-128.5	-47.8	-3263	-1214
043	D7	-128.5	-53.4	-3263	-1357
044	N.C.	-128.5	-59.0	-3263	-1499
045	D8	-128.5	-64.6	-3263	-1642
046	D9	-128.5	-70.2	-3263	-1784
047	V_{CCP}	-128.5	-75.9	-3263	-1927
048	V_{SS}	-128.5	-81.5	-3263	-2069
049	V_{CC}	-128.5	-87.1	-3263	-2212
050	V_{SS}	-128.5	-92.7	-3263	-2354
051	V_{SS}	-128.5	-98.3	-3263	-2497
052	D10	-128.5	-103.9	-3263	-2639
053	D11	-128.5	-109.5	-3263	-2782
054	D12	-128.5	-115.1	-3263	-2924
055	D13	-128.5	-120.7	-3263	-3067
056	V_{CC}	-128.5	-126.3	-3263	-3209
057	V_{SS}	-128.5	-132.0	-3263	-3352
058	V_{CCP}	-128.5	-137.6	-3263	-3494
059	V_{SS}	-128.5	-143.2	-3263	-3637
060	D14	-128.5	-148.8	-3263	-3779
061	D15	-128.5	-154.4	-3263	-3922
062	N.C.	-128.5	-160.0	-3263	-4064
063	D16	-128.5	-165.6	-3263	-4207
064	V_{SS}	-128.5	-171.2	-3263	-4349
065	V_{CCP}	-128.5	-176.8	-3263	-4492
066	V_{SS}	-128.5	-182.4	-3263	-4634
067	V_{SS}	-115.1	-194.5	-2923	-4939

Table 1. Embedded Ultra-Low Power Intel486™ SX Processor Bond Pad Center Data (Sheet 3 of 7)

PAD#	SIGNAL[2,3,4,5]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
068	D17	-109.5	-194.5	-2781	-4939
069	V_{CC}	-103.9	-194.5	-2638	-4939
070	D18	-98.3	-194.5	-2496	-4939
071	D19	-92.6	-194.5	-2353	-4939
072	D20	-87.0	-194.5	-2211	-4939
073	V_{SS}	-81.4	-194.5	-2068	-4939
074	V_{CCP}	-75.8	-194.5	-1926	-4939
075	D21	-70.2	-194.5	-1783	-4939
076	D22	-64.6	-194.5	-1641	-4939
077	D23	-59.0	-194.5	-1498	-4939
078	N.C.	-53.4	-194.5	-1356	-4939
079	V_{CCP}	-47.8	-194.5	-1213	-4939
080	V_{SS}	-42.1	-194.5	-1071	-4939
081	D24	-36.5	-194.5	-928	-4939
082	D25	-30.9	-194.5	-786	-4939
083	D26	-25.3	-194.5	-643	-4939
084	D27	-19.7	-194.5	-501	-4939
085	V_{SS}	-14.1	-194.5	-358	-4939
086	V_{CCP}	-8.5	-194.5	-216	-4939
087	V_{CC}	-2.4	-194.5	-62	-4939
088	V_{SS}	3.2	-194.5	81	-4939
089	D28	8.8	-194.5	223	-4939
090	D29	14.4	-194.5	366	-4939
091	D30	20.0	-194.5	508	-4939
092	D31	25.6	-194.5	651	-4939
093	STPCLK#[6]	31.5	-194.5	799	-4939
094	V_{SS}	37.1	-194.5	942	-4939
095	V_{CC}	42.7	-194.5	1084	-4939
096	TDO	48.3	-194.5	1227	-4939
097	SMI#	57.8	-194.5	1467	-4939
098	V_{SS}	63.4	-194.5	1609	-4939
099	V_{CCP}	69.0	-194.5	1752	-4939
100	V_{SS}	74.6	-194.5	1894	-4939
101	V_{CC}	80.2	-194.5	2037	-4939

Table 1. Embedded Ultra-Low Power Intel486™ SX Processor Bond Pad Center Data (Sheet 4 of 7)

PAD#	SIGNAL[2,3,4,5]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
102	SMIACT#	85.8	-194.5	2179	-4939
103	SRESET	91.4	-194.5	2322	-4939
104	NMI	97.0	-194.5	2464	-4939
105	INTR	102.6	-194.5	2607	-4939
106	FLUSH#	108.2	-194.5	2749	-4939
107	V_{SS}	113.9	-194.5	2892	-4939
108	V_{SS}	128.5	-176.8	3263	-4492
109	RESET	128.5	-171.2	3263	-4349
110	A20M#	128.5	-165.6	3263	-4207
111	EADS#	128.5	-160.0	3263	-4064
112	V_{SS}	128.5	-154.4	3263	-3922
113	V_{CC}	128.5	-148.8	3263	-3779
114	V_{SS}	128.5	-143.2	3263	-3637
115	V_{CCP}	128.5	-137.6	3263	-3494
116	PCD	128.5	-132.0	3263	-3352
117	PWT	128.5	-126.3	3263	-3209
118	D/C#	128.5	-120.7	3263	-3067
119	M/IO#	128.5	-115.1	3263	-2924
120	N.C.	128.5	-109.5	3263	-2782
121	V_{SS}	128.5	-103.9	3263	-2639
122	V_{CC}	128.5	-98.3	3263	-2497
123	BE3#	128.5	-92.7	3263	-2354
124	BE2#	128.5	-87.1	3263	-2212
125	BE1#	128.5	-81.5	3263	-2069
126	BE0#	128.5	-75.9	3263	-1927
127	BREQ	128.5	-70.2	3263	-1784
128	V_{SS}	128.5	-64.6	3263	-1642
129	V_{CC}	128.5	-59.0	3263	-1499
130	V_{SS}	128.5	-53.4	3263	-1357
131	V_{CCP}	128.5	-47.8	3263	-1214
132	W/R#	128.5	-42.2	3263	-1072
133	HLDA	128.5	-36.6	3263	-929
134	CLK	128.5	-31.0	3263	-787
135	V_{SS}	128.5	-25.4	3263	-644

Table 1. Embedded Ultra-Low Power Intel486™ SX Processor Bond Pad Center Data (Sheet 5 of 7)

PAD#	SIGNAL[2,3,4,5]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
136	V_{CC}	128.5	-19.7	3263	-502
137	V_{SS}	128.5	-14.1	3263	-359
138	V_{CC}	128.5	-8.5	3263	-217
139	V_{SS}	128.5	-2.9	3263	-74
140	V_{CC}	128.5	2.7	3263	68
141	V_{SS}	128.5	8.3	3263	211
142	V_{CC}	128.5	13.9	3263	353
143	N.C.	128.5	19.5	3263	496
144	TCK	128.5	25.1	3263	638
145	AHOLD	128.5	30.7	3263	781
146	HOLD	128.5	36.4	3263	923
147	V_{SS}	128.5	42.0	3263	1066
148	V_{CC}	128.5	47.6	3263	1208
149	KEN#	128.5	53.2	3263	1351
150	RDY#	128.5	58.8	3263	1493
151	N.C.	128.5	64.4	3263	1636
152	V_{SS}	128.5	70.0	3263	1778
153	V_{CC}	128.5	75.6	3263	1921
154	BS8#	128.5	81.2	3263	2063
155	BS16#	128.5	86.8	3263	2206
156	BOFF#	128.5	92.5	3263	2348
157	BRDY#	128.5	98.1	3263	2491
158	N.C.	128.5	103.7	3263	2633
159	N.C.	128.5	109.3	3263	2776
160	V_{SS}	128.5	114.9	3263	2918
161	V_{CC}	128.5	120.5	3263	3061
162	V_{SS}	128.5	126.1	3263	3203
163	V_{CCP}	128.5	131.7	3263	3346
164	LOCK#	128.5	139.6	3263	3545
165	PLOCK#	128.5	145.2	3263	3688
166	V_{SS}	128.5	150.8	3263	3830
167	V_{CC}	128.5	156.4	3263	3973
168	BLAST#	128.5	164.3	3263	4172
169	ADS#	128.5	169.9	3263	4315

Table 1. Embedded Ultra-Low Power Intel486™ SX Processor Bond Pad Center Data (Sheet 6 of 7)

PAD#	SIGNAL[2,3,4,5]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
170	A2	128.5	175.5	3263	4457
171	V_{SS}	128.5	181.1	3263	4600
172	V_{CCP}	128.5	186.7	3263	4742
173	V_{CCP}	116.6	194.5	2962	4939
174	V_{SS}	111.0	194.5	2819	4939
175	A3	104.6	194.5	2658	4939
176	A4	99.0	194.5	2515	4939
177	A5	93.4	194.5	2373	4939
178	RESERVED[7]	87.8	194.5	2230	4939
179	A6	82.2	194.5	2088	4939
180	A7	76.6	194.5	1945	4939
181	A8	71.0	194.5	1803	4939
182	V_{SS}	61.5	194.5	1562	4939
183	V_{CCP}	55.9	194.5	1420	4939
184	V_{SS}	50.3	194.5	1277	4939
185	V_{CC}	44.7	194.5	1135	4939
186	A9	39.1	194.5	992	4939
187	A10	33.5	194.5	850	4939
188	V_{SS}	27.8	194.5	707	4939
189	V_{CC}	22.2	194.5	565	4939
190	V_{SS}	16.6	194.5	422	4939
191	V_{CCP}	11.0	194.5	280	4939
192	V_{SS}	5.4	194.5	137	4939
193	V_{CC}	-0.2	194.5	-5	4939
194	A11	-6.3	194.5	-159	4939
195	N.C.	-11.9	194.5	-302	4939
196	A12	-17.5	194.5	-444	4939
197	V_{SS}	-23.1	194.5	-587	4939
198	V_{CC}	-28.7	194.5	-729	4939
199	A13	-34.3	194.5	-872	4939
200	A14	-39.9	194.5	-1014	4939
201	V_{SS}	-45.5	194.5	-1157	4939
202	V_{CCP}	-51.1	194.5	-1299	4939
203	A15	-56.8	194.5	-1442	4939

Table 1. Embedded Ultra-Low Power Intel486™ SX Processor Bond Pad Center Data (Sheet 7 of 7)

PAD#	SIGNAL[2,3,4,5]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
204	A16	-62.4	194.5	-1584	4939
205	A17	-68.0	194.5	-1727	4939
206	V_{SS}	-73.6	194.5	-1869	4939
207	V_{CCP}	-79.2	194.5	-2012	4939
208	TDI	-84.8	194.5	-2154	4939
209	TMS	-90.4	194.5	-2297	4939
210	A18	-96.0	194.5	-2439	4939
211	A19	-101.6	194.5	-2582	4939
212	A20	-107.3	194.5	-2724	4939
213	V_{SS}	-112.9	194.5	-2867	4939
214	V_{CCP}	-118.5	194.5	-3009	4939

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol "#" is used to denote active low signals.
4. V_{CCP} refers to the I/O interface (pad) supply voltage while V_{CC} refers to the CPU core supply voltage. Voltages differ. See datasheet #272731 for supply voltage rules.
5. Boundary Scan (JTAG) is implemented through the following pads: 96 (TDO), 144 (TCK), 208 (TDI), 209 (TMS).
6. The STPCLK# signal (Pad 093) must be tied to V_{CCP} through a 10 KΩ resistor if left unused.
7. RESERVED Pad 178 must be tied to V_{CCP} through a 10 KΩ resistor.

2.0 INTEL DIE PRODUCTS PROCESSING

2.1 Test Procedure

Intel has instituted full-speed functional testing at the die level for all SmartDie products. This level of testing is ordinarily performed only after assembly into a package. Each die is tested to the same electrical limits as the equivalent packaged unit.

2.2 Wafer Probe

Wafer probing is performed on every wafer produced in Intel Fabs. The process consists of specific electrical tests and device-specific functionality tests.

At the wafer level, built-in test structures are probed to verify that device electrical characteristics are in control and meet specifications. Measurements are made of transistor threshold voltages and current characteristics; poly and contact resistance; gate oxide and junction integrity; and specific parameters critical to the particular technology and device type. Wafer-to-wafer, across-the-wafer run-to-run variation and conformance to spec limits are checked.

The actual devices on each wafer are then probed for both functionality and performance to specifications. Additional reliability tests are also included in the probe steps.

2.3 Wafer Saw

Probed wafers are transferred to Intel's assembly sites to be sawed. The saw cuts totally through the wafer.

2.4 Die Inspection

Upon completion of the wafer saw, the die are moved to pick and place equipment that removes reject die. The remaining die are submitted to the same visual inspection as standard packaged product. The compliant die are then transferred to GEL-PAKs for shipment.

2.5 Packing Procedure

Intel will ship all Intel die products in GEL-PAKs. GEL-PAKs eliminate the die edge damage usually associated with die cavity plates or chip trays.

The backside of each die adheres to the gel membrane in the GEL-PAK, eliminating the risk of damage to the active die surface. A simple vacuum release mechanism allows for pick and place removal at the customer's site.

Only die from the same wafer lot are packaged together in a GEL-PAK, and all die are placed in the GEL-PAKs with a consistent orientation. The GEL-PAKs are then sealed and labeled with the following information:

- Intel SmartDie
- Intel Part Number
- Assembly Process Order / Spec
- ROM Code (if applicable)
- Customer Part Number (if applicable)
- Assembly Lot Traveler Number
- Finished Product Order Number
- Quantity
- Seal Date
- Country of Origin

NOTE:

GEL-PAKs require a Vacuum Release Station. Contact Vichem* Corporation for more information.

2.6 Inspection Steps

Multiple inspection steps are performed during the die fabrication and packing flow. These steps are performed according to the same specifications and criteria established for Intel's standard packaged product. Specific inspection steps include a wafer saw visual as well as a final die visual just before die are sealed in moisture barrier bags.

2.7 Storage Requirements

Intel die products will be shipped in GEL-PAKs and sealed in a moisture-barrier anti-static bag with a desiccant. No special storage procedures are required while the bag is still unopened. Once opened, the GEL-PAK should be stored in a dry, inert atmosphere to prevent corrosion of the bond pads.

2.8 Electro-Static Discharge (ESD)

Components are ESD sensitive.

3.0 SPECIFICATIONS

Specifications within this document are specific to a particular die revision and are subject to change without notice. Verify with your local Intel Sales Office that you have the latest data before finalizing a design.

3.1 Physical Specifications

Table 2 defines Embedded Ultra-Low Power Intel486™ SX processor physical specifications.

Table 2. Embedded Ultra-Low Power Intel486™ SX Processor Physical Specifications

Die Revision:	B-0
Post-Saw Die Dimensions:	X = 271 ± 0.5, Y = 402 ± 0.5 See Figure 2 for X, Y orientation.
Die Thickness:	17 ± 1.0 mils
Minimum Pad Pitch:	Pads may not be evenly pitched. Minimum pitch is: 142.5 microns (5.6 mils)
Pad Passivation Opening Size:	Mils: 4.6 x 4.6 Microns: 118.7 x 118.7
Bond Pad Metallization: (outermost layer first)	1 Micron Aluminum (0.5% Copper), 0.1 microns Titanium
Pads per Die:	214
Die Backside Material: (outermost layer first)	1500 ± 500 Angstroms Gold, 200 ± 100 Angstroms Chrome
Passivation: (outermost layer first)	5 microns Polyimide, 0.6 microns Nitride
Intel Fabrication Process:	CHMOS V (min. feature size 0.8 microns)

3.2 DC Specifications

ABSOLUTE MAXIMUM RATINGS†

GEL-PAK Storage Temperature ..... 0°C to +70°C
Junction Temperature Under Bias ..... -65°C to +110°C
Supply Voltage V_{CC} wrt V_{SS} ..... -0.5 V to +4.6 V
Supply Voltage V_{CCP} wrt V_{SS} ..... -0.5 V to +4.6 V

OPERATING CONDITIONS†

T_J (Junction Temperature Under Bias) ..... 0°C to 90°C
Substrate Bias ..... V_{SS}
Voltage:

NOTICE: This document contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice. Verify with your local Intel Sales Office that you have the latest data before finalizing a design.

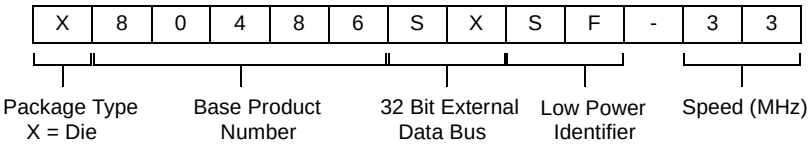
†***WARNING:*** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

V_{CCP} Range(1)	Max. CLK Freq.	V_{CC} Range(2)	V_{CC} Fluctuation
3.3 V ± 0.3 V	25 MHz	2.4 V min 3.3 V max	±0.2 V at 2.4 V≤V_{CC}≤2.7 V +0.3 V / -0.2 V at 2.7 V<V_{CC}<3.0 V
	33 MHz	2.7 V min 3.3 V max	0.3 V at 3.0 V≤V_{CC}≤3.3 V

NOTES:

1. In all cases, V_{CCP} must be ≥ V_{CC}.
2. V_{CC} may be set to any voltage within the V_{CC} Range. The setting determines the allowed V_{CC} Fluctuation.

4.0 DEVICE NOMENCLATURE



VALID COMBINATION:
X80486SXSF-33

5.0 REFERENCE INFORMATION

Document Title	Order #
Intel486™ Microprocesor Family datasheet	242202
Intel486™ Microprocesor Hardware Reference Manual	240552
Intel486™ Microprocesor Family Programmer's Reference Manual	240486
Embedded Ultra-Low Power Intel486™ SX Processor datasheet	272731
Embedded Ultra-Low Power Intel486™ GX Processor datasheet	272755

6.0 REVISION HISTORY

Revision	Date	Description
001	3/96	Initial Release