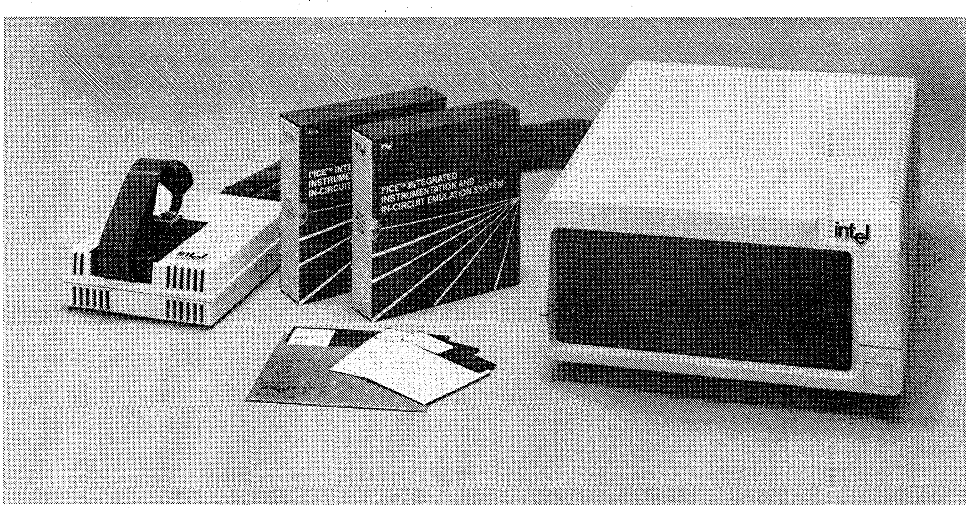
intel®

I²ICE™ Integrated Instrumentation and In-Circuit Emulation System

- **Provides Real-Time In-Circuit Emulation**
- **Offers Symbolic Debugging Capabilities**
  - **— Accesses Memory Locations and Program Variables (Including Dynamic Variables) Using Program-Defined Names**
  - **— Maintains a Virtual Symbol Table**
- **Offers Multi-Condition, Multi-Level, Multi-Probe Break and Trace Capability**
- **Provides Built-In AEDIT Editor to Allow Editing of Development System Files without Exiting from I²ICE Operation**
- **Provides Low Cost Conversions Among 8086, 8088, 80186, 80188 and 80286 Microprocessors**
- **Simultaneously Controls up to Four Microprocessors for Debugging Multiprocessor Systems for a Single Work Station**
- **Supports Common Memory between Processor without Any User System Hardware**
- **Offers an Integrated 16-Channel 100-MHz Logic Timing Analyzer**
- **Maps User Program Memory into a Maximum of 288K Zero-Wait-State RAM (Zero Wait-States up to 10 MHz)**
- **Maps User I/O to Console or to Debugging Procedures**
- **Provides Disassembly and Single-Line Assembly to Help with On-Line Code Patching**
- **Common Human Interface Provided by the PSCOPE-86 Debugging Language and the I²ICE Command Language**
- **Uses Integrated Command Directory, ICD™, for Command Syntax Direction/Correction to Ease Debug Operations**

The Intel Integrated Instrumentation and In-Circuit Emulation (I²ICE™) system aids the design of systems that use the 8086, 8088, 80186, 80188, and 80286 microprocessors. The I²ICE system combines symbolic software debugging, in-circuit emulation, and the optional Intel Logic Timing Analyzer (iLTA). Support features for the 8087 and 80287 coprocessors are also included. For the 8086/8088, 80186/80188, and 80286 processors, the I²ICE system support programs written in "C", PL/M, FORTRAN, Pascal, Ada*, and assembly language. Up to four I²ICE system instrumentation chassis can be hosted by one of Intel's Intellec® microcomputer development systems or by an IBM PC AT or PC XT.



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*Ada is a trademark of the Joint Ada Program Office. U.S. Department of Defense.

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PHYSICAL DESCRIPTION

The I2ICE system hardware consists of the host interface board, the I2ICE system instrumentation chassis, the emulation base module, the emulation personality module, a host/chassis cable, interchassis cables (for multiple chassis systems), a user cable, optional high-speed memory boards, and an optional logic timing analyzer. The I2ICE system software consists of I2ICE system host software, I2ICE system probe software, confidence tests, PSOPE 86, and optional iLTA software. Table 1 shows elements of the I2ICE system.

The host interface board resides in the host development system. A cable connects the host interface board to the I2ICE system instrumentation chassis. Another cable connects the I2ICE system instrumentation chassis to the buffer box.

The instrumentation chassis contains high-speed zero-wait-state emulation memory, break-and-trace logic, memory and I/O maps, and the emulation clips assembly.

The chassis may also contain the optional logic timing analyzer and optional high-speed memory. High-speed memory is expandable from 32K bytes to 288K bytes in 128K increments.

The buffer box contains the emulation personality module. This module configures the I2ICE system for a particular iAPX microprocessor. The user cable connects the buffer box to user prototype hardware.

The host development system may host up to four I2ICE system instrumentation chassis. Each chassis may have its own buffer box, user cable, emulation clips, optional high-speed memory boards, and logic timing analyzer.

FUNCTIONAL DESCRIPTION

Resource Borrowing

The I2ICE system memory map allows the prototype system to borrow memory resources from the I2ICE system.

If prototype memory is not yet available, the user program may reside in I2ICE system memory. Because this memory is RAM, changes can be made quickly and easily. For example, if the prototype contains EPROM, it does not need to be erased and reprogrammed during development.

Later, as prototype memory becomes available, the verified user program can be reassigned, memory block by memory block to prototype memory.

The I2ICE™ System Memory Map

The I2ICE system can direct (map) an emulated microprocessor's memory space (the user program memory) to any combination of the following:

- High-speed I2ICE system memory—this consists of 32K bytes of programamble wait-state memory (programmable from 0 to 15). This memory resides in the I2ICE system chassis on the map-I/O board.
- Optional high-speed I2ICE system memory—this consists of up to 256K bytes of programmable wait-state memory (0 wait-states up to 10 MHz). This memory resides in the I2ICE system chassis on one or two optional high-speed memory boards (128 K bytes each).
- MULTIBUS® bus memory (host system memory)—this resides in the host development system itself. (Any amount of unused host memory can be used in 1K increments.) Note that this feature is not available for a PC host.
- User memory—this resides in the user prototype hardware.

When a user program runs in I2ICE system memory or user memory, the I2ICE system emulates in real time. A memory access to MULTIBUS bus memory, however, inserts approximately 25 wait-states into the memory cycle.

Access Restrictions

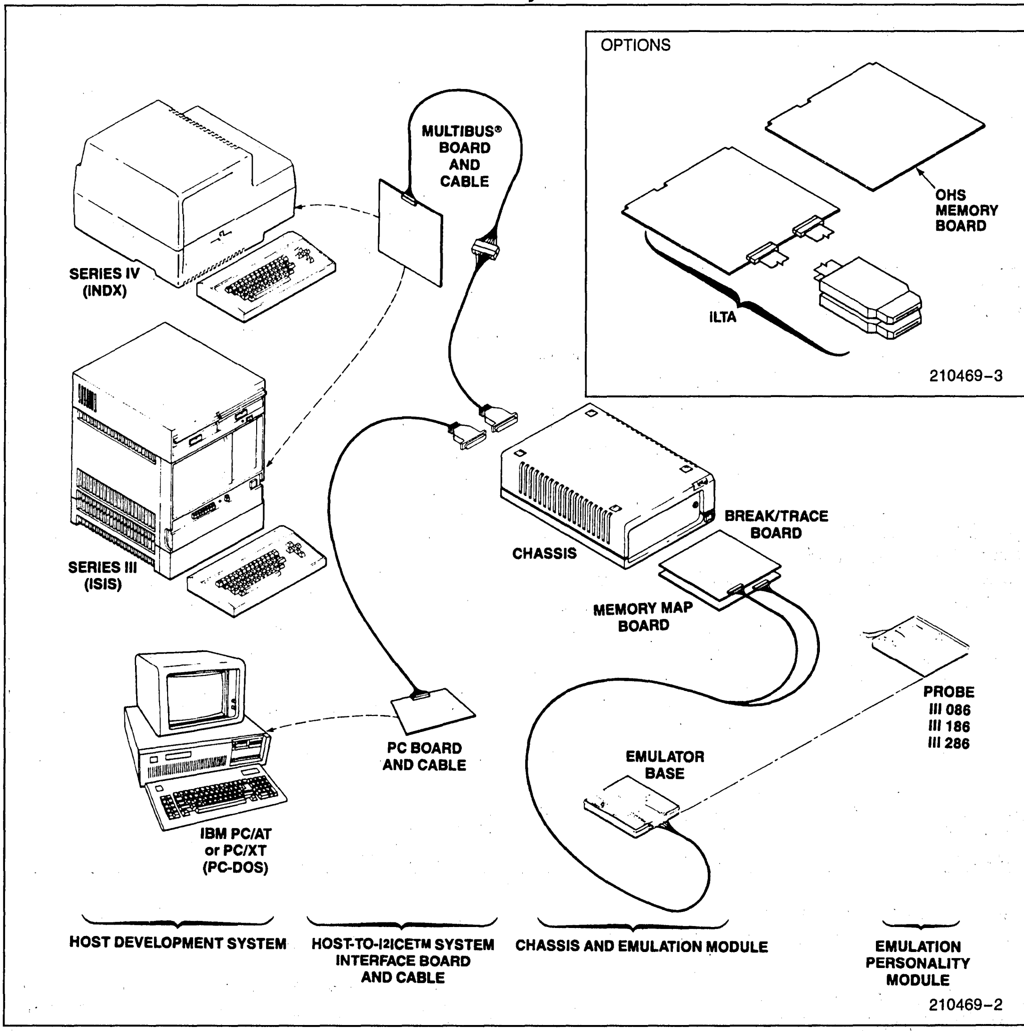
In addition to directing memory accesses, the following access restrictions can be specified:

- Read-only—the I2ICE system displays an error message if a user program attempts to write to an area of memory designated as read-only. The user can, however, write to a read-only area with I2ICE system commands.
- Read/write, no verify—normally, the I2ICE system performs a read-after-write verification after program loads and after writing to memory with an I2ICE system command. The I2ICE system can suppress this verification. For example, if a prototype has memory-mapped I/O, a verifying read may change the state of the I/O device.
- Guarded—initially, the I2ICE system puts all memory in a guarded state. Neither the user program nor the I2ICE system user can access guarded memory.

The I2ICE™ System I/O Map

The I2ICE system can direct (map) an emulated microprocessor's I/O space to the host development

Table 1. I2ICE™ System Overview



Name	Description
Host Development System	Required for all applications. Use one of the following: • Intellec Series III development system • Intellec Series IV development system • IBM PC AT or PC XT (with 512K bytes of available memory and version 3.0 of PC DOS) • IBM 50 system (available in Japan; features *kanji*)

Table 1. I2ICE™ System Overview (Continued)

Name	Description
Host-to-I2ICE System Interface Board, Cable, and Host Software	Required for communication between the host and the I2ICE system. • MULTIBUS® bus interface board for Series III and Series IV (product code III520) • Host-to-I2ICE system cable for Series III and Series IV (product code III530 or III531) • I2ICE system host software for the Series III and Series IV (product code III951A, B, or C) • Package with PC host interface board, cable and PC DOS version of I2ICE host software (product code III520AT954D)
Instrumentation Chassis and Emulation Module	Required for real-time microprocessor emulation, break and trace capability, and memory and i/O capability. • Instrumentation chassis (product code III514B) has four board slots: 1 slot for break/trace board 1 slot for map-I/O board 2 slots for 1 (or 2) optional high-speed memory board(s) and/or 1 optional logic timing analyzer board • Maximum of four chassis for multi-probe applications • Emulation module (product code III620) includes break/trace board, map-I/O board, and buffer base box
Emulation Personality Module (Probe) and Probe Software	Required for emulation of specific microprocessors: 8086/8088, 80186/80188, or 80286. • Module includes personality board, buffer box cover, and user cable • Series III or IV: Order probe and probe software separately • PC host: Probe and probe software packaged together
Logic Timing Analyzer (iLTA) [not shown]	Required for acquisition and storage of events and glitches for signal measurement applications. • Complete with iLTA board (mounts in instrumentation chassis), probe pods, and cables • User Series III or Series IV host (cannot be used with the IBM PC AT and PC XT)
Optional High-Speed Memory Board (OHS) [not shown]	Required for memory expansion. • 128K bytes of programmable (0 to 15) wait-state memory • One or two boards mount in the instrumentation chassis

system's console, to the prototype system, to debugging procedures, or to a combination of these.

SIMULATING I/O WITH THE HOST DEVELOPMENT CONSOLE

Suppose a user program requires input from an I/O device not yet part of the prototype. Map the input port range assigned to that device to the host development systems' console. Then, when the user program requires input, it halts and the I2ICE system console displays a message requesting the data. When you enter the required data at the keyboard, the user program continues.

SIMULATING I/O WITH I2ICE™ SYSTEM DEBUGGING PROCEDURES

Procedures that supply the needed input data can be written in the I2ICE system command language. When setting up the I/O map, the user specifies that the I/O procedure is invoked when certain I/O ports are accessed.

I/O ports are mapped in blocks of 64 byte-wide ports or 32 word-wide ports. A total of 64K byte-wide ports or 32K word-wide ports can be mapped.

Symbolic Debugging

With symbolic debugging, a memory location can be referenced by specifying its symbolic reference. A symbolic reference is a procedure name, line number, or label in the user program that corresponds to a location in the user program's memory space.

TYPICAL SYMBOLIC FUNCTIONS

Symbolic functions include:

- Changing or inspecting the value and type of a program variable by using its program-defined name, rather than the address of the memory location where the variable and a hexadecimal value for the data are stored.
- Defining break and trace events using source-code symbols.

With symbolic debugging, the user can reference static variables, dynamic (stack-resident) variables, based variables, and record structures combining primitive data types. The primitive data types are ADDRESS, BOOLEAN, BYTE BCD, CHAR, WORD, DWORD, SELECTOR, POINTER, three INTEGER Types, and four REAL types.

THE VIRTUAL SYMBOL TABLE

The I2ICE system maintains a virtual symbol table for program symbols; that is, the entire symbol table need not fit into memory at the same time. (The size of the virtual symbol table is constrained only by the capacity of the storage device.)

The I2ICE system divides the symbol table into pages. If a program's symbol table is large, the I2ICE system reads only some of the symbol table pages into memory. When the user references a variable whose symbol is not currently defined in memory, the I2ICE system reads the needed symbol table page from disk into memory.

Breakpoint, Trace, and Arm Specifications

With I2ICE system commands, breakpoint, trace, and arm specifications can be defined.

Breakpoints allow halting of a user program in order to examine the effect of the program's execution on the prototype. With the I2ICE system, a breakpoint can be set at a particular memory location or at a particular statement in a user program (including high-level language programs). A break can also be set to occur when the user program enters or accesses a specified memory partition or reads or writes a user program variable. When the user program resumes execution, it picks up from where it left off.

Normally, the I2ICE system traces while the user program executes. With a trace specification, however, the user can choose to have tracing occur only when specific conditions are met.

An arm specification describes an event or combination of events that must occur before the I2ICE system can recognize certain breakpoint and trace specifications. Typical events are the execution of an instruction or the modification of a data value.

The I2ICE system command language allows you to specify complex, multilevel events. For example, you can specify that a break occurs when a variable is written, but only if that write occurs within a certain procedure. The execution of the procedure is the arm condition; the variable modification is the break condition. The I2ICE system command language allows users to specify complex events with up to four states with four conditions and to use such events as arm, break, or trace conditions; a specified number of events can be used as a condition.

Coprocessor Support

The 8086/8088 emulation personality module provides transparent RQ/GT and MN/MX pin emulation to support real-time prototype systems that use the 8087 as a coprocessor. The 8086/8088 (and the 80186/80188) emulation personality module also provides debugging features specific to the 8087. I2ICE system commands provide access to the 8087's stack, status registers, and flags. The I2ICE system's disassembly and trace features extend to 8087 instructions and data types.

The 80186 and 80286 emulation personality modules also allow the prototype hardware to contain coprocessors. The 80186 probe can qualify break points and collect trace information when the coprocessor drives the status lines ($\overline{S0}$–$\overline{S2}$) in the prescribed manner. The 80286 personality module allows the hardware to contain the 80287 processor extension and provides special debugging features—the user can enable and disable the 80287 and change and examine its registers.

DUBUGGING WITH THE I2ICE™ SYSTEM

The I2ICE system allows both hardware and software debugging (see Figure 1).

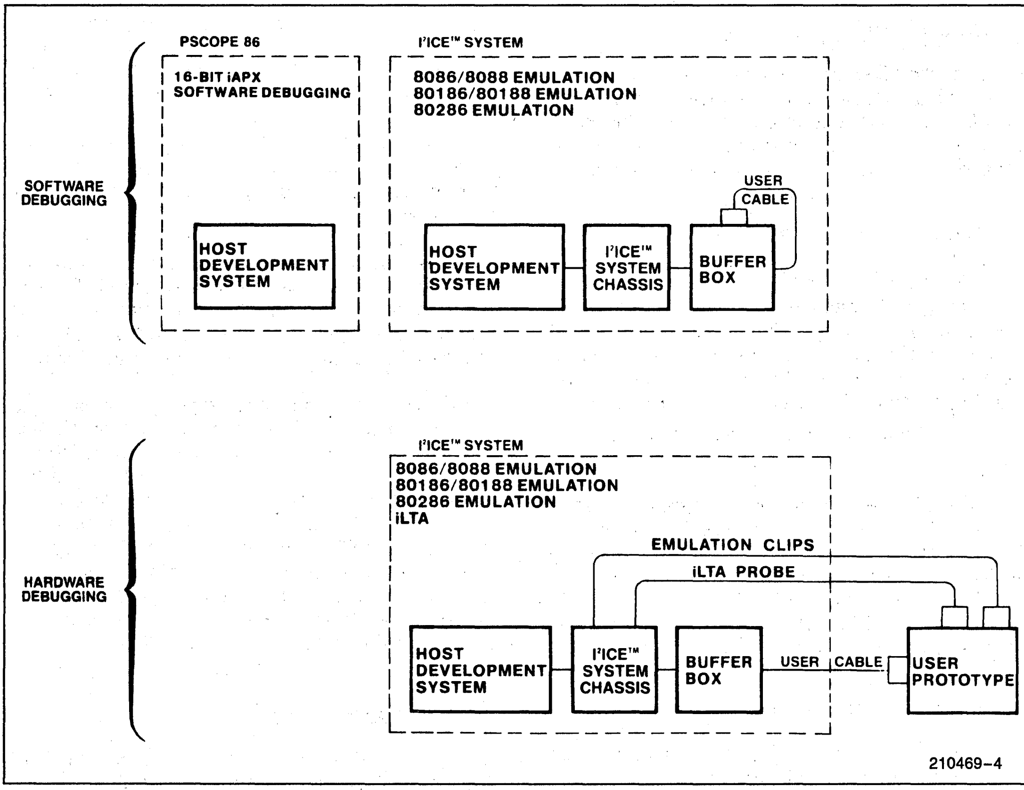


Figure 1. I²ICE™ System Debugging Capabilities

- Software debugging—I²ICE system commands permit symbolic debugging of user programs written in high-level languages as well as assembly language. By looping the user cable back into the buffer box, a user program can be debugged even if no prototype hardware is present. In a multi-probe environment, the I²ICE system can map common memory from the host development system and support semaphore operation even with no user system prototype hardware. This feature makes possible detailed debugging of multi-processor software before the hardware is available.
- Hardware debugging—the I²ICE system is a real-time, in-circuit emulator. Trace data are collected in real time, and I²ICE system software does not intrude into user program space. The optional iLTA adds the high-speed timing and data acquisition of a logic timing analyzer.

The userfulness of an I²ICE system extends throughout the development cycle, beginning with the symbolic debugging of prototype software and ending with the final integration of debugged software and prototype hardware.

PSCOPE 86

PSCOPE 86 is a high-level language, symbolic debugger, designed for use with Pascal 86, PL/M 86, and FORTRAN 86. It is a separate product included with Series III and Series IV versions of the I²ICE system; it runs in the host development system. PSCOPE 86 is field-proven, familiar to Intel customers, and suited for the debugging of applications software when the hardware capabilities of the I2ICE system are not needed. The PSCOPE 86 and I2ICE system command languages are similar. (Note that PSCOPE 86 is available as an option for use with the PC AT or PC XT.)

Designing a product that contains a microcomputer requires close coordination of hardware and software development. A typical design process takes advantage of both the I2ICE system and PSCOPE 86. Use PSCOPE 86 for debugging software before downloading the software into a target environment; use the I2ICE system for debugging and emulation in the target system.

THE I2ICE™ SYSTEM COMMAND LANGUAGE

The syntax of I2ICE system commands resembles that of a high-level language. The I2ICE system command langauge is versatile and powerful while remaining easy to learn and use.

The Integrated Command Directory (ICD™) assists users with command syntax.

- The ICD directory directs the user in choosing commands from display on the bottom line of the screen. As commands are entered, the bottom line indicates syntax elements available for use in the commands.
- The ICD directory flags syntax errors. Syntax errors are flagged as they occur (rather than after the carriage return is pressed).
- The ICD directory provides on-line help with the HELP command.

Automatic expansion of LITERALLY expressions is available. When the feature is activated, each character string defined by a LITERALLY definition is automatically expanded to its full length.

The I2ICE system command language deals with user-created, debugging objects. By manipulating debugging objects, the user can streamline complex debugging sessions.

Debugging objects are uniquely named, user-created, software constructs that the I2ICE system uses to manage the debugging environment. The four types of debugging objects are: debugging procedures, LITERALLY definitions, debugging registers, and debugging variables. In the following examples, I2ICE system keywords are shown in all caps.

- Debugging procedures (named groups of I2ICE system commands) can simulate missing software or hardware, collect debugging information, and make troubleshooting decisions. For example, consider a debugging procedure (called **init**) that simulates input from I/O ports 2 and 4.

  The procedure and MAPIO command are given first, followed by an explanation.

```
*DEFINE PROCEDURE init = DO
.*IF %0 = = 2 THEN
..*PORTDATA = 100T
..*ELSE IF %0 = = 4 THEN
...*PORTDATA = 65T ...*END
..*END
.*END
*MAPIO 0 LENGTH 64K ICE (init)
```

  Whenever the MAPIO command maps I/O ports to an I2ICE system procedure, three parameters are made available to the procedure (even if the procedure does not use them): %0, %1, %2. The parameter %0 passes the port number; %1 passes a Boolean value that indicates whether read or write I/O activity will occur; and %2 passes a Boolean value that indicates whether the I/O is a byte-wide or a word-wide port. PORTDATA is a pseudo-variable that contains the actual port data. This procedure specifies that if port 2 is used, the procedure returns 100 (base ten); if, however, port 4 is used, the procedure returns 65 (base ten).
- LITERALLY definitions are shorthand names for previously defined character strings. LITERALLY definitions can save keystrokes and improve clarity. For example, here is the definition of a LITERALLY that saves keystrokes. This LITERALLY allows the user to type DEF for DEFINE.

```
*DEFINE LITERALLY DEF = "DEFINE"
```

  These definitions may be saved to disk and autoreloaded. In addition, an automatic LITERALLY expansion feature can be turned on and off.
- Debugging registers are user-created, software registers that hold arm, breakpoint, and trace specifications. The I2ICE system can be ordered to emulate the user program and specify one or more debugging registers. There is no need to reenter the specificatoin for each emulation. For example here is the definition of a debugging register called **pay** that contains a trace specification. This example takes advantage of the previous LITERALLY definition.

```
*DEF TRCREG pay = :cmaker.payment
```

To emulate a user program and trace only during the procedure **payment,** specify the debugging register **pay** as part of the GO command.

```
*GO USING pay
```

- Debugging variables are user-created variables used with I^{2}ICE system commands. For example, here is the definition of a debugging variable called **begin.** Its type is POINTER.

```
*DEFINE POINTER begin = 0020H:0006H
```

During a debugging session, the user can set the execution point to this pointer value by typing:

```
*$ = begin
```

The I^{2}ICE system pseudo-variable $ represents the current execution point.

Example of a Debugging Session

Figures 2, 3, and 4 illustrate some of the key capabilities of the I^{2}ICE system. The user program is written in Pascal-86. It was compiled, linked, and located on an Intellec Series III development system. The resulting file consists of absolute code and is called CMAKER.86. Figure 2 shows the Pascal listing; Figure 3 shows a sample debugging session; and Figure 4 briefly explains the debugging steps shown in Figure 3.

The CMAKER.86 program controls an automatic changemaker. The program reads the amount tendered (the variable **paid**) and the amount of the purchase (the variable **purchase**). It calculates the coins needed for change and asserts control signals to a change release mechanism by writing an output port. Each of the lower four bits of the output port controls the release of a different coin denomination.

3			0
Q	D	N	P

Q = quarters
D = dimes
N = nickels
P = pennnies

I^{2}ICE™ System Command Functions

The I^{2}ICE system command language contains a number of functional categories.

- Emulation commands—the GO command instructs the I^{2}ICE system to begin emulation. The user can also command the I^{2}ICE system to break or trace under certain specified conditions.
- Utility commands—these are general purpose commands for use in a debugging environment. For example, one use of the EVAL command is to calculate the nearest source-code line number that corresponds to the address of an assembly language instruction. The HELP command provides on-line assistance. The EDIT command invokes a menu-driven text editor (AEDIT) that allows updating of debugging object definitions and editing of development system files without exiting from the I^{2}ICE system. A command line editior and history key are also provided.
- Environment commands—these are commands that set up the debugging environment. For example, the MAP command sets up the memory map. Another environment command (WAITSTATE) inserts wait-states into memory accesses, allowing the simulation of slow memories.
- File handling commands—these are commands that access disk files. Debugging object definitions can be saved in a disk file and loaded in later debugging sessions. Debugging sessions can also be recorded in a disk file for later analysis.
- Probe-specific commands—these are commands whose effects are different for different probes. For example, the PINS command displays the state of selected signals lines on the current probe.
- Option-specific commands—these are commands that control an optional test/measurement device, such as the logic timing analyzer.

I^{2}ICE™ SYSTEM INSTRUMENTATION SUPPORT

I^{2}ICE™ System Emulation Clips

Eight external input lines are sampled during each processor bus cycle. The I^{2}ICE system records the values of these lines in it trace buffer during each execution cycle. The I^{2}ICE system can use these values when defining events.

Four additional output lines synchronize I^{2}ICE system events with external hardware. Two lines are active and programmable with I^{2}ICE system commands. Two other lines, break and trace, allow an I^{2}ICE system chassis to be linked to other I^{2}ICE system chassis.

Intel Logic Timing Analyzer (iLTA)

The iLTA analyzer is a chassis-resident, test/measurement module designed to extend the capability of the I^{2}ICE system to recognize events and collect data. The iLTA and the I^{2}ICE system emulator work together. They can trigger and arm/disarm each other. In addition, waveforms acquired by the

```
SERIES-III Pascal-86, V2.0
Source File: CMAKER.SRC
Object File: CMAKER.OBJ
Controls Specified: XREF, DEBUG, TYPE

STMT  LINE  NESTING    SOURCE TEXT: MAKER.SRC
  1     1    0  0      PROGRAM cmaker;
  2     2    0  0      VAR change,coins                                 :integer;
  3     3    0  0         quarters,nickels,dimes,pennies                :integer;
  4     4    0  0         paid,purchase                                 :word;

  5     6    0  0      PROCEDURE payment;
  6     7    1  0         VAR numberofcoins                             :integer;
  7     8    1  0            release                                    :word;
  8     9    1  0         BEGIN    (*payment*)
  8    10    1  1         numberofcoins:=quarters+dimes+nickels+pennies;
  9    11    1  1            while numberofcoins< >0 do
 10    12    1  1            BEGIN
 10    13    1  2            release:=0;
 11    14    1  2            if quarters< >0 then
 12    15    1  2               BEGIN
 12    16    1  3               release:=release+8;
 13    17    1  3               quarters:=quarters-1
                               END;

 15    19    1  2            if dimes< >0 then
 16    20    1  2               BEGIN
 16    21    1  3               release:=release+4;
 17    22    1  3               dimes:=dimes-1
                               END;
 19    24    1  2            if nickels< >0 then
 20    25    1  2               BEGIN
 20    26    1  3               release:=release+2;
 21    27    1  3               nickels:=nickels-1
                               END;
 23    29    1  2            if pennies< >0 then
 24    30    1  2               BEGIN
 24    31    1  3               release:=release+1;
 25    32    1  3               pennies:=pennies-1
                               END;
 27    34    1  2            numberofcoins:=quarters+dimes+nickels+pennies;
 28    35    1  2            OUTWRD(130,release);
 29    36    1  2            END;
 31    37    1  1         END;     (*payment*)

 32    39    0  0      BEGIN   (*main*)
 32    40    0  1      INWRD(2,paid);
 33    41    0  1      INWRD(70,purchase);
 34    42    0  1      change   :=paid-purchase;
 35    43    0  1      coins    :=change mod 100;
 36    44    0  1      quarters: =coins div 25;
 37    45    0  1      coins    :=coins mod 25;
 38    46    0  1      dimes    :=coins div 10;
 39    47    0  1      coins    :=coins mod 10;
 40    48    0  1      nickels  :=coins div 5;
 41    49    0  1      pennies  :=coins mod 5;
 42    50    0  1      payment;
 43    51    0  1      END.     (*main*)
```

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Figure 2. Listing of CMAKER.86

```
(1)  *BASE
     DECIMAL
(2)  *MAP 0K LENGTH 32K HS
     *MAPIO 0T LENGTH 192T ICE
     *MAP
     MAP          0K LENGTH     32K HS
     MAP         32K LENGTH    992K GUARDED
     *MAPIO
     MAPIO 00000H LENGTH       000C0H ICE
     MAPIO 000C0H LENGTH       0FF40H USER
(3)  *LOAD :F1:CMAKER.86
(4)  *DEFINE POINTER begin = $
     *DEFINE BRKREG pay = :cmaker #9
     *DEFINE PROC display = DO
     .*WRITE USING (' "quarters = ",T,0,>')quarters
     .*WRITE USING (' "dimes = ",T,0')dimes
     .*WRITE USING (' "nickels = ",T,0,>')nickels
     .*WRITE USING (' "pennies = ",T,0')pennies
     .*RETURN TRUE
     .*END
(5)  *GO USING pay
     ?UNIT 0 PORT 2H REQUESTS WORD INPUT (ENTER VALUE)*100
     ?UNIT 0 PORT 46H REQUESTS WORD INPUT (ENTER VALUE)*65
     Probe 0 stopped at :CMAKER #9 + 4 because of execute break
       Break register is PAY Trace Buffer Overflow
(6)  *quarters;dimes;numberofcoins
     +1
     +1
     +2
(7)  *DEFINE SYSREG wr_number = WRITE AT .:cmaker.payment.numberofcoins &
     **CALL display
     *GO USING wr_number
       quarters = + 1    dimes = +1
       nickels = +0      pennies = +0
     Probe 0 stopped at :CMAKER # 28 + 3 because of bus break
       Break register is WR_NUMBER
(8)  *numberofcoins
     +0
     *EVAL release
     1100Y 12T CH'..'
(9)  *CLIPSOUT = 11Y
(10) *GO FOREVER
     ?UNIT 0 PORT 82H OUTPUT WORD 0C
     ?Probe 0 stopped at location 0033:00AEH because of bus not active
       Bus address = 0203DE
     *$ = begin
     *
```

Figure 3. Sample Debugging Session (Explanations in Figure 4)

(1) Checking to see that the default radix is decimal.

(2) Mapping user program memory to I²ICE high-speed memory and user I/O ports to the I²ICE system console.

(3) Loading the user program.

(4) Defining debugging objects.

The debugging variable **begin** is set to $, an I²ICE pseudo-variable representing the current execution point. At this point is the debugging session, $ is the beginning of the user program.

The break register **pay** specifies a breakpoint at statement 9 in the user program.

The debuggning procedure **display** displays the value of some user program variables on the console.

(5) Beginning emulation with the debugging register **pay.** The console requests the two input values, **paid** and **purchase.** Then, the break occurs.

(6) Displaying three user program variables.

(7) Defining another debugging register. The specified event is the writing of the user program variable **numberofcoins.** When that event occurs, the I²ICE system calls the debugging procedure **display.** In addition to displaying some user program variables, this debugging procedure returns a Boolean value. Because this value is TRUE, the break occurs; if the value were FALSE, emulation would continue.

(8) Displaying the two user program variables, **numberofcoins** and **release.** The EVAL command displays **release** in binary, decimal, hexadecimal, and ASCII. Unprintable ASCII characters appear as periods (.).

(9) Asserting both output lines on the emulation clips. These lines are input to the prototype hardware and control a change release mechanism.

(10) Resuming emulation. The console displays the write of **release** to the output port. The user program finishes exeucting, and the probe stops emulating because of bus inactivity. The $ is set back to the beginning of the user program in preparation for another emulation.

Figure 4. Explanation of Sample Debugging Session in Figure 3

iLTA can be time-aligned with I²ICE system traces. (Note that iLTA is not available for use with the PC AT or PC XT.)

The iLTA analyzer brings the flexibility of high-speed triggering and glitch detection to the I²ICE system. The iLTA is a general purpose logic timing analyzer, supplemented with special features for microsystem debugging and I²ICE system integration. Following are some of iLTA's features.

- 16-channel, 100 MHz asynchronous operation
- 16-channel, 50 MHz asynchronous operation
- Single- or double-height timing waveforms presented with data scrolling, magnification, and delta-time read-out features.
- Minimum 3 nanosecond glitch detection (3 ns + 1 ns/volt for signal swings greater than 3 volts)
- A dual-threshold acquisition mode, with programmable logic level thresholds.
- A burst acquisition mode with window boundary indicators.
- User-defined channel labels and state display radixes.
- Disk storage for preservation and restoration of analyzer setups and acquired waveforms.
- Logic waveform comparison features (compares current acquisitions with pervious traces stored in auxiliary memory or on disk).

- Menu-driven operation and user-friendly display. The display takes advantage of screen highlighting, blinking characters, and reverse video.
- Powerful post-processing data analysis commands that are part of the I²ICE system command language.
- Multiple emulator break/trace and iLTA trigger/trace conditions may be shared with as many as four emulators and four iLTAs.

I²ICE™ SYSTEM SPECIFICATIONS

Host Requirements

Series III, Series IV, Model 800, or IBM PC AT or PC XT.

512K bytes in host development system memory space.

Two double-density diskette drives or a hard disk.

For the iLTA to run on a Series III, the III-820 board must be installed. Model 800 systems and the IBM PC AT and PC XT systems do not support the iLTA option.

I²ICE™ System Software

I²ICE system host software
I²ICE system probe software
I²ICE system confidence tests
I²ICE tutorial
PSCOPE 86 (not currently available for PC-DOS)
Optional iLTA software and iLTA confidence tests (not available for PC-DOS)

System Performance

Mappable zero wait-state memory (zero wait-states up to 10 MHz for 8086; 8 MHz for 8088 and 80186/80188; and 6 or 8 MHz for 80286):	Minimum 32K bytes, maximum 288K bytes
Trace buffer:	1023 x 48 bits
Virtual symbol table:	The number of user program symbols is limited only by available disk space

Physical Characteristics

INSTRUMENTATION CHASSIS
Width: 17.0 in (43.2 cm)
Height: 8.25 in (21.0 cm)
Depth: 24.13 in (61.3 cm)
Weight: 48 lbs (21.9 kg)

HOST/CHASSIS CABLE

10 ft (3.0m) and 40 ft (12.2 m) options for Series III/Series IV host
15 ft (4.6m) for PC host

INTER-CHASSIS CABLE SET

2 ft (61 cm) and 10 ft (3.0m) options

BUFFER BOX
Width: 8.5 in (21.6 cm)
Height: 3.0 in (7.6 cm)
Depth: 10.0 in (25.4 cm)
Weight: 8 lbs (3.7 kg)

Electrical Characteristics

90–132V or 180–264V (selectable)
47–63 Hz
12 amps (AC)

Environmental Requirements

Operating Temperature:	0°C to 40°C (32°F to 104°F)
Operating Humidity:	Maximum of 85% relative humidity, non-condensing

Emulation Clips

Emulation clipsin lines are sampled once every bus cycle when the address bits become valid on the address bus. During emulation, the I2ICE system records the value of the clipsin lines in the trace buffer once very execution cycle.

Table 2. I2ICE™ Emulation Clips—DC Characteristics

Signal	Input Voltage		Input Current		Output Current	
	Low V_{IL} V	High V_{IH} V	Low I_{IL} μA	High I_{IH} μA	Low I_{OL} mA	High OH mA
Clipsout Lines					33 at 0.7V	4.8 at 2.0V
SYSBREAK SYSTRACE					38 at 0.7V	1.0 at 2.0V
Clipsin Lines	1.05	2.5	50	50		

I2ICE™ SYSTEM 8086/8088 PROBE HIGHLIGHTS

- Provides up to 10 MHz real-time emulation
- One-megabyte addressing
- Emulates both Minimum and Maximum modes
- Provides 8087 coprocessor support

Table 3. I2ICE™ System 8086/8088 User Interface—DC Characteristics

Signal	Input Voltage		Output Voltage		Input Current		Output Current			
	Max V_{IL} V	Min V_{IH} V	Max V_{OL} V	Min V_{OH} V	Max I_{IL} mA	Max I_{IH} mA	Max I_{OL} mA	Max I_{OH} mA	3-State Max I_{OZL} mA	3-State Max I_{OZH} mA
AD15–AD0	0.8	2.0	0.5	2.0	−0.20	0.02	24	−12.0	−0.20	0.02
A19–A16, $\overline{BHE}$/S7	0.8	2.0	0.55	2.0	−0.25	0.07	63.9	−15.0	−0.07	0.07
$\overline{RD}$	NA	NA	0.55	2.0	NA	NA	63.9	−15.0	−0.84	0.05
$\overline{DEN}$ ($\overline{S0}$), DT/$\overline{R}$ ($\overline{S1}$), M/$\overline{IO}$ ($\overline{S2}$)	0.8	2.0	0.55	2.0	−1.20	0.12	18.8	−6.6	−1.30	0.12
$\overline{WR}$ ($\overline{LOCK}$)	NA	NA	0.55	2.0	NA	NA	63.9	−15.0	−0.94	−0.05
$\overline{INTA}$ (QS1)	NA	NA	0.5	2.4	NA	NA	19.1	−6.50	NA	NA
ALE (QS0)	NA	NA	0.5	2.4	NA	NA	19.9	−6.54	NA	NA
MN/$\overline{MX}$	0.8	2.0	NA	NA	−1.6	0.04	NA	NA	NA	NA
NMI	0.77	2.0	NA	NA	−0.4	0.05	NA	NA	NA	NA
CLK, READY*	0.8	2.0	NA	NA	−3.2	0.04	NA	NA	NA	NA
INTR	0.77	2.0	NA	NA	−0.4	0.05	NA	NA	NA	NA
$\overline{TEST}$	0.8	2.0	NA	NA	−0.60	0.04	NA	NA	NA	NA
RESET	0.8	2.0	NA	NA	−2.2	0.07	NA	NA	NA	NA
HOLD ($\overline{RQ}/\overline{GT0}$), HOLDA ($\overline{RQ}/\overline{GT1}$)	0.72	2.0	0.80	2.0	−1.60	−0.11	7.60	−7.06	NA	NA

***NOTES:**
I_{IL} = −0.8 mA and I_{IH} = 0.1 mA if a 74S244 is used at U30 for CLOCK and READY inputs.

Negative currents (−) are defined as currents flowing out of a terminal, and positive currents are defined as currents flowing into a terminal. "NA" means "not applicable."

The 8086 and 8088 chip specifications indicate that the chips have an output drive capacity of I_{OH} = − 400 μA and I_{OL} = 2.5 mA (2.0 mA for the 8088); the chips' input and 3-state loading specification is ±10 μA. As can be seen from the table, the 8086/8088 probe has a greater output drive capacity and presents greater input loading than the 8086 or 8088 chip.

The 8086/8088 probe does not draw any current from the user V_{CC}.

Capacitive Loading—8086/8088 Probe

- The 8086/8088 probe presents the user system with a maximum load of 70 pF (135 pF for INTR, NMI).
- All 8086/8088 probe outputs are capable of driving 0 pF while meeting all the probe's timing specifications. The 8086/8088 probe will drive larger capacitive loads, but with possible performance degradation. Derate the timing specifications by 0.04 ns/pF corresponding to input capacitance of the user system.

Coprocessor Operation—8086/8088 Probe

- During emulation with external coprocessors, a two-clock delay precedes each $\overline{RQ}$, $\overline{GT}$, and RLS pulse in MAX mode and each HOLD and HOLDA assertion in MIN mode.
- The user can choose to have the coprocessor run only during emulation or all the time. If the coprocessor runs all the time, then during interrogation mode,the coprocessor may have as much as a one-microsecond delay in addition to the two-clock delay mentioned above.
- The I2ICE system ignores a coprocessor when the probe is in the reset state. If a coprocessor asserts $\overline{RQ}$ during this time, the $\overline{RQ}/\overline{GT}$ sequence may get out of synchronization. The probe is reset when the I2ICE host software loads I2ICE probe software.

A.C. CHARACTERISTICS FOR THE I2ICE™ SYSTEM 8086 PROBE

Tables 4 through 7 provide timing information for the 8086 probe. Figures 5 through 12 define the timing symbols.

Table 4. Minimum Complexity System Timing Requirements

Min Mode Symbol	Parameter	5 MHz (8086)		10 MHz (8086-1)		8 MHz (8086-2)	
		Min ns	Max ns	Min ns	Max ns	Min ns	Max ns
TCLCL	CLK Cycle Period	200	500	100	500	125	500
TCLCH	CLK Cycle Low Time	118		53		68	
TCHCL	CLK High Time	69		39		44	
TCH1CH2	CLK Rise Time		10		10		10
TCL2CL1	CLK Fall Time		10		10		10
TDVCL(1)	Data in Setup Time	21.1		21.1(5)		21.1(20)	
TCLDX(2)	Data in Hold Time	13.5(10)		13.5(10)		13.5(10)	
TR1VCL(3, 4)	RDY Hold Time into 8284A	35		35		35	
TCLR1X(3, 4)	RDY Hold Time into 8284A	0		0		0	
TRYHCH(5)	READY Setup Time into 8086	44.5		44.5		44.5	
TCHRYX(6)	READY Hold Time into 8086	20.5		20.5(20)		20.5(20)	
TRYLCL(5)	READY Inactive to CLK	−18.5		−18.5		−18.5	
THVCH(1)	HOLD Setup Time	12.7		12.7		12.7	
TINVCH NMI(1) INTR(1) $\overline{TEST}$(1)	INTR, NMI, $\overline{TEST}$ Setup Time	50.5 + TCLCH(30) 20 21.5		50.5 + TCLCH(15) 20(15) 21.5(150		50.5 + TCLCH(15) 20(15) 21.5(15)	
TILIH	Input Rise Time (Except CLK)		20		20		20
TIHIL	Input Fall Time (Except CLK)		12		12		12

Numbers followed by parentheses deviate from the 8086 chip specification; the 1985 *Microsystem Components Handbook* chip specification timing is given in the parentheses.

NOTES:
1. Timings are calculated with a 74F244 as the buffer for CLOCK or READY. If a 74S244 is used, add 0.7 ns to the timings.
2. Timings are calculated with a 74F244 as the buffer for CLOCK or READY. If a 74S244 is used, add 2.5 ns to the timings.
3. The signal at 8284 is for reference only.
4. The setup requirement, for asynchronous signal is only to guarantee recognition at the next CLK.
5. If BTHRDY = TRUE, READY must be set up 0.3 ns before the rising edge of T2.
6. If BTHRDY = TRUE, READY must be held 16.5 ns after the rising edge of T2.

A.C. CHARACTERISTICS FOR THE I2ICE™ SYSTEM 8086 PROBE (Continued)

Table 5. Minimum Complexity System Timing Responses

Min Mode Symbol	Parameter	5 MHz (8086)		10 MHz (8086-1)		8 MHz (8086-2)	
		Min ns	Max ns	Min ns	Max ns	Min ns	Max ns
TCLAV(1)	Address Valid Delay	17.5	64.5	17.5	64.5(50)	17.5	64.5(60)
TCLAX(2)	Address Hold Time	17.5		17.5		17.5	
TCLAZ(1)	Address Float Delay	14.6	61.5	14.6	61.5(40)	14.6	61.5(50)
TLHLL	ALE Width	TCLCH−17.5 (TCLCH−20)		TCLCH−17.5		TCLCH−17.5	
TCLLH(1)	ALE Active Delay		42		42(40)		42
TCHLL(1)	ALE Inactive Delay		35		35		35
TLLAX	Address Hold Time to ALE Inactive	TCHCL−8.5		TCHCL−8.5		TCHCL−8.5	
TCLDV(1)	Data Valid Delay	17.5	69.5	17.5	69.5(50)	17.5	69.5(60)
TCHDX(2)	Data Hold Time	17.5		17.5		17.5	
TWHDX	Data Hold Time after $\overline{WR}$	TCLCH−34 (TCLCH−30)		TCLCH−34 (TCLCH−25)		TCLCH−34 (TCLCH−30)	
TCVCTV $\overline{DEN}$(READ, INTA)(1)	Control Active Delay(1)	15.6	63.5	15.6	63.5(50)	15.6	63.5
$\overline{DEN}$($\overline{WR}$)(1)		TCHCL+15.6	TCHCL+63.5 (110)	TCHCL+15.6	TCHCL+63.5 (50)	TCHCL+15.6	TCHCL+63.5 (70)
$\overline{WR}$(1)		16.9	59.5	16.9	59.5(50)	16.9	59.5
INTA(1)		15.9	55	15.9	55(50)	15.9	55
TCHCTV M/$\overline{IO}$(1, 3)	Control Active Delay 2	19	77	19	77(45)	19	77(60)
DT/$\overline{R}$(1, 4)		18.4	73.5	18.4	73.5(45)	18.4	73.5(60)
TCVCTX $\overline{DEN}$(1)	Control Inactive Delay	15.6	63.5	15.6	63.5(50)	15.6	63.5
$\overline{WR}$(1)		16.9	59.5	16.9	59.5(50)	16.9	59.5
INTA(1)		15.9	55	15.9	55(50)	15.9	55
TAZRL	Address Float to READ Active	−37.2(0)		−37.2(0)		−37.2(0)	
TCLRL(1)	$\overline{RD}$ Active Delay	15.9	80.5	15.9	80.5(70)	15.9	80.5
TCLRH(1)	$\overline{RD}$ Inactive Delay	15.9	70.5	15.9	70.5(60)	15.9	70.5
TRHAV	$\overline{RD}$ Inactive to Next Address Active	(Note 5)		(Note 5)		(Note 5)	
TCLHAV(1)	HLDA Valid Delay	11.3	57	11.3	57	11.3	57
TRLRH	$\overline{RD}$ Width	2TCLCL−52.5		2TCLCL−52.5 (2TCLCL−40)		2TCLCL−52.5 (2TCLCL−50)	
TWLWH	$\overline{WR}$ Width	2TCLCL−27.5		2TCLCL−27.5		2TCLCL−27.5	
TAVAL	Address Valid to ALE Low	TCLCH−47.2		TCLCH−47.2 (TCLCH−35)		TCLCH−47.2 (TCLCH−40)	
TOLOH	Output Rise Time		20		20		20
TOHOL	Output Fall Time		12		12		12

Numbers followed by parenthese deviate from the 8086 chip specification; the 1985 *Microsystem Components Handbook* chip specification timing is given in the parentheses.

NOTES:
1. Timings are calculated with a 74F244 as the buffer for CLOCK or READY. If a 74S244 is used, add 2.5 ns to the timings.
2. Timings are calculated with a 74F244 as the buffer for CLOCK or READY. If a 74S244 is used, add 0.7 ns to the timings.
3. When performing consecutive I/O cycles (i.e., word I/O to an odd address), the M/IO line goes high for a short time during T4. The 8086 microprocessor keeps M/IO low between consecutive I/O cycles.
4. When performing consecutive reads to program memory, the DT/$\overline{R}$ line of the probe microprocessor (at the end of the user cable) goes high for a short time between reads. The 8086 microprocessor keeps DR/$\overline{R}$ low between consecutive reads.
5. The address data lines are only floated during T4 when $\overline{RD}$ is active.

A.C. CHARACTERISTICS FOR THE I²ICE™ SYSTEM 8086 PROBE (Continued)

Table 6. Maximum Complexity System Timing Requirements

Min Mode Symbol	Parameter	5 MHz (8086)		10 MHz (8086-1)		8 MHz (8086-2)	
		Min	Max ns	Min ns	Max ns	Min ns	Max ns
TCLCL	CLK Cycle Period	200	500	100	500	125	500
TCLCH	CLK Low Time	118		60(53)		68	
TCHCL	CLK High Time	69		39		44	
TCH1CH2	CLK Rise Time		10		10		10
TCL2CL1	CLK Fall Time		10		10		10
TDVCL(1)	Data in Setup Time	21.1		21.1(5)		21.1(20)	
TCLDX(2)	Data in Hold Time	13.5(10)		13.5(10)		13.5(10)	
TR1VCL(3, 4)	RDY Setup Time into 8284A	35		35		35	
TCLR1X(3, 4)	RDY Hold Time into 8284A	0		0		0	
TRYHCH(5)	READY Setup Time into 8086	44.5		44.5		44.5	
TCHRYX(6)	READY Hold Time into 8086	20.5		20.5(20)		20.5(20)	
TRYLCL(5)	READY Inactive to CLK	−18.5		−18.5		−18.5	
TINVCH NMI(1) INTR(1) TEST(1)	Setup Time for Recognition (INTR, NMI, TEST)	50.5 + TCLCH(30) 20 21.5		50.5 + TCLCH(15) 20(15) 21.5(15)		50.5 + TCLCH(15) 20(15) 21.5(15)	
TGVCH(1)	RQ/GT Setup Time	12.7		12.7(12)		12.7	
TCHGX(2)	RQ Hold Time into 8086	16.1	16.1			16.1	
TILIH	Input Rise Time (Except CLK)		20		20		20
TIHIL	Input Fall Time (Except CLK)		12		12		12

Numbers followed by parentheses deviate from the 8086 chip specification; the 1985 *Microsystem Components Handbook* chip specification timing is given in the parentheses.

NOTES:
1. Timings are calculated with a 74F244 as the buffer for CLOCK or READY. If a 74S244 is used, add 0.7 ns to the timings.
2. Timings are calculated with a 74F244 as the buffer for CLOCK or READY. If a 74S244 is used, add 2.5 ns to the timings.
3. The signal at 8284 or 8288 is for reference only.
4. The setup requirement, for asynchronous signal is only to guarantee recognition at the next CLK.
5. If BTHRDY = TRUE, READY must be set up 0.3 ns before the rising edge of T2.
6. If BTHRDY = TRUE, READY must be held 16.5 ns after the rising edge of T2.

A.C. CHARACTERISTICS FOR THE I2ICE™ SYSTEM 8086 PROBE (Continued)

Table 7. Maximum Complexity System Timing Responses

Min Mode Symbol	Parameter	5 MHz (8086)		10 MHz (8086-1)		8 MHz (8086-2)	
		Min ns	Max ns	Min ns	Max ns	Min ns	Max ns
TCLML(1)	Command Active Delay	10	35	10	35	10	35
TCLMH(1)	Command Inactive Delay	10	35	10	35	10	35
TRYHSH(2, 3, 4)	READY Active to Status Passive		37.5		37.5		37.5
TCHSV(4)	Status Active Delay	17	66.5	17	66.5(45)	17	66.5(60)
TCLSH(4)	Status Inactive Delay	10.5	42.5	10.5	42.5	10.5	42.5
TCLAV(4)	Address Valid Delay	17.5	64.5	17.5	64.5(50)	17.5	64.5(60)
TCLAX(5)	Address Hold Time	17.5(10)		17.5(10)		17.5(10)	
TCLAZ(4)	Address Float Delay	14.6	61.5	14.6	61.5(40)	14.6	61.5(50)
TSVLH(1)	Status Valid to ALE High		15		15		15
TSVMCH(1)	Status Valid to MCE High		15		15		15
TCLLH(1)	CLK Low to ALE Valid		15		15		15
TCLMCH(1)	CLK Low to MCE High		15		15		15
TCHLL(1)	ALE Inactive Delay		15		15		15
TCLMCL(1)	MCE Inactive Delay		15		15		15
TCLDV(4)	Data Valid Delay	17.5	69.5	17.5	69.5(50)	17.5	69.5(60)
TCHDX(5)	Data Hold Time	17.5		17.5		17.5	
TCVNV(1)	Control Active Delay	5	45	5	45	5	45
TCVNX(1)	Control Inactive Delay	10	45	10	45	10	45
TAZRL	Address Float to Read Active	−37.2(0)		−37.2(0)		−37.2(0)	
TCLRL(4)	$\overline{RD}$ Active Delay	15.9	80.5	15.9	80.5(70)	15.9	80.5
TCLRH(4)	$\overline{RD}$ Inactive Delay	15.9	70.5	15.9	70.5(60)	15.9	70.5
TRHAV	$\overline{RD}$ Inactive to Next Address Active	(Note 6)		(Note 6)		(Note 6)	
TCHDTL(1)	Direction Control Active Delay		50		50		50
TCHDTH(1)	Direction Control Inactive Delay		30		30		30
TCLGL(4)	$\overline{GT}$ Active Delay	12.9	54.5	12.9	54.5(45)	12.9	54.5(50)
TCLGH(4)	$\overline{GT}$ Inactive Delay	14.9	65	14.9	65(45)	14.9	65(50)
TRLRH	$\overline{RD}$ Width	2TCLCL−52.5		2TCLCL−52.5 (2TCLCL−40)		2TCLCL−52.5 (2TCLCL−50)	
TOLOH	Output Rise Time		20		20		20
TOHOL	Output Fall Time		12		12		12

Numbers followed by parentheses deviate from the 8088 chip specification; the 1985 *Microsystem Components Handbook* chip specification timing is given in the parentheses.

NOTES:
1. The signal at 8284 or 8288 is for reference only.
2. If BTHRDY = TRUE, READY must be set up 0.3 ns before the rising edge of T2.
3. For BTHRDY = TRUE, TRYHSH = TRYHCH + 47.
4. Timings are calculated with a 74F244 as the buffer for CLOCK or READY. If a 74S244 is used, add 2.5 ns to the timings.
5. Timings are calculated with a 74F244 as the buffer for CLOCK or READY. If a 74S244 is used, add 0.7 ns to the timings.
6. The address data lines are only floated during T4 when RD is active.

A.C. CHARACTERISTICS FOR THE I2ICE™ SYSTEM 8088 PROBE

Tables 8 through 11 provide timing information for the 8088 probe. Figures 5 through 12 define the timing symbols.

Table 8. Minimum Complexity System Timing Requirements

Min Mode Symbol	Parameter	5 MHz (8088)		8 MHz (8088-1)	
		Min ns	Max ns	Min ns	Max ns
TCLCL	CLK Cycle Period	200	500	125	500
TCLCH	CLK Low Time	118		68	
TCHCL	CLK High Time	69		44	
TCH1CH2	CLK Rise Time		10		10
TCL2CL1	CLK Fall Time		10		10
TDVCL(1)	Data in Setup Time	21.1		21.1(20)	
TCLDX(2)	Data in Hold Time	13.5(10)		13.5(10)	
TR1VCL(3, 4)	RDY Setup Time into 8284	35		35	
TCLR1X(3, 4)	RDY Hold Time into 8284	0		0	
TRYHCH(5)	READY Setup Time into 8088	57.8		57.8	
TCHRYX(6)	READY Hold Time into 8088	20.5		20.5(20)	
TRYLCL(5)	READY Inactive to CLK	−16.5		−16.5	
THVCH(1)	Hold Setup Time	12.7		12.7	
TINVCH NMI(1)	INTR, NMI, $\overline{TEST}$ Setup Time	50.5 + TCLCH(30)		50.5 + TCLCH(15)	
INTR(1)		26		26(15)	
$\overline{TEST}$(1)		27.5		27.5(15)	
TILIH	Input Rise Time		20		20
TIHIL	Input Fall Time		12		12

Numbers followed by parentheses deviate from the 8088 chip specification; the 1985 *Microsystem Components Handbook* chip specification timing is given in the parentheses.

NOTES:
1. Timings are calculated with a 74F244 as the buffer for CLOCK or READY. If a 74S244 is used, add 0.7 ns to the timings.
2. Timings are calculated with a 74F244 as the buffer for CLOCK or READY. If a 74S244 is used, add 2.5 ns to the timings.
3. The signal at 8284 is for reference only.
4. The setup requirement, for asynchronous signal is only to guarantee recognition at the next CLK.
5. For BTHRDY = TRUE, READY must be set up 0.3 ns prior to the rising edge of T2.
6. For BTHRDY = TRUE, READY must be held 16.5 ns after the rising edge of T2.

A.C. CHARACTERISTICS FOR THE I2ICE™ SYSTEM 8088 PROBE (Continued)

Table 9. Minimum Complexity System Timing Responses

Min Mode Symbol	Parameter	5 MHz (8088)		8 MHz (8088-2)	
		Min ns	Max ns	Min ns	Max ns
TCLAV[1]	Address Valid Delay	17.5	72	17.5	72(60)
TCLAX[2]	Address Hold Time	17.5		17.5	
TCLAZ[1]	Address Float Delay	13.6	61.5	13.6	61.5(50)
TLHLL	ALE Width	TCLCH − 17.5 (TCLCH − 20)		TCLCH − 17.5	
TCLLH[1]	ALE Active Delay		41		41
TCHLL[1]	ALE Inactive Delay		35		35
TLLAX	Address Hold Time to ALE Inactive	TCHCL − 8.5		TCLCH − 8.5	
TCLDV[1]	Data Valid Delay	17.5	70.5	17.5	70.5(60)
TCHDX[2]	Data Hold Time	17.5		17.5	
TWHDX	Data Hold Time after $\overline{WR}$	TCLCH − 34 (TCLCH − 30)		TCLCH − 34 (TCLCH − 30)	
TCVCTV $\overline{DEN(RD,}$ INTA)[1] $\overline{DEN}$(WRITE)[1] $\overline{WR}$[1] INTA[1]	Control Active Delay 1	 15.6 TCHCL + 13.6 16.9 15.9	 63.5 TCHCL + 63.5 (110) 59.5 55	 15.6 TCHCL + 13.6 16.9 15.9	 63.5 TCHCL + 63.5 (70) 59.5 55
TCHCTV SS0[1] IO/$\overline{M}$[1, 3] DT/$\overline{R}$[1, 4]	Control Inactive Delay 2	 16.3 19.1 18.3	 104 81 77.5	 16.3 19.1 18.3	 104(60) 81(60) 77.5(60)
TCVCTX $\overline{DEN}$[1] $\overline{WR}$[1] INTA[1]	Control Inactive Delay	 15.6 16.9 15.9	 63.5 59.5 55	 15.6 16.9 15.9	 63.5 59.5 55
TAZRL	Address Float to READ Active	−37.2(0)		−37.2(0)	
TCLRL[1]	$\overline{RD}$ Active Delay	15.9	110.5	15.9	110.5(100)
TCLRH[1]	$\overline{RD}$ Inactive Delay	15.9	90.5	15.9	90.5(80)
TRHAV	$\overline{RD}$ Inactive to Next Address Active	(Note 5)		(Note 5)	
TCLHAV[1]	HLDA Valid Delay	13.3	57	13.3	57
TRLRH	$\overline{RD}$ Width	2TCLCL − 82.5 (2TCLCL − 75)		2TCLCL − 82.5 (2TCLCL − 50)	
TWLWH	$\overline{WR}$ Width	2TCLCL − 27.5		2TCLCL − 27.5	
TAVAL	Address Valid to ALE Low	TCLCH − 52.2		TCLCH − 52.2 (TCLCH − 40)	
TOLOH	Output Rise Time		20		20
TOHOL	Output Fall Time		12		12

Numbers followed by parentheses deviate from the 8088 chip specification; the 1985 *Microsystem Components Handbook* chip specification timing is given in the parentheses.

NOTES:
1. Timings are calculated with a 74F244 as the buffer for CLOCK or READY. If a 74S244 is used, add 2.5 ns to the timings.
2. Timings are calculated with a 74F244 as the buffer for CLOCK or READY. If a 74S244 is used, add 0.7 ns to the timings.
3. When performing consecutive I/O cycles (i.e., word I/O to an odd address), the M/IO line goes high for a short time during T4. The 8088 microprocessor keeps IO/M low between consecutive I/O cycles.
4. When performing consecutive reads to program memory, the DT/$\overline{R}$ line of the probe microprocessor (at the end of the user cable) goes high for a short time between reads. The 8088 microprocessor keeps DR/$\overline{R}$ low between consecutive reads.
5. The address data lines are only floated during T4 when $\overline{RD}$ is active.

A.C. CHARACTERISTICS FOR THE I2ICE™ SYSTEM 8088 PROBE (Continued)

Table 10. Maximum Complexity System Timing Requirements

Min Mode Symbol	Parameter	5 MHz (8088)		8 MHz (8088-2)	
		Min ns	Max ns	Min ns	Max ns
TCLCL	CLK Cycle Period	200	500	125	500
TCLCH	CLK Low Time	118		68	
TCHCL	CLK High Time	69		44	
TCH1CH2	CLK Rise Time		10		10
TCL2CL1	CLK Fall Time		10		10
TDVCL(1)	Data in Setup Time	21.1		21.1(20)	
TCLDX(2)	Data in Hold Time	13.5(10)		13.5(10)	
TR1VCL(3, 4)	RDY Setup Time into 8284	35		35	
TCLR1X(3, 4)	RDY Hold Time into 8284	0		0	
TRYHCH(5)	READY Setup Time into 8088	57.8		57.8	
TCHRYX(6)	READY Hold Time into 8088	20.5		20.5(20)	
TRYLCL(5)	READY Inactive to CLK	−16.5		−16.5	
TINVCH NMI(1)	Setup Time for Recognition (INTR, NMI, $\overline{TEST}$)	50.5 + TCLCH(30)		50.5 + TCLCH(15)	
INTR(1)		26		26(15)	
$\overline{TEST}$(1)		27.5		27.5(15)	
TGVCH(1)	$\overline{RQ}/\overline{GT}$ Setup Time	12.7		12.7	
TCHGX(2)	$\overline{RQ}$ Hold Time into 8088	16.1		16.1	
TILIH	Input Rise Time (Except CLK)		20		20
TIHIL	Input Fall Time (Except CLK)		12		12

Numbers followed by parentheses deviate from the 8088 chip specification; the 1985 *Microsystem Components Handbook* chip specification timing is given in the parentheses.

NOTES:
1. Timings are calculated with a 74F244 as the buffer for CLOCK or READY. If a 74S244 is used, add 0.7 ns to the timings.
2. Timings are calculated with a 74F244 as the buffer for CLOCK or READY. If a 74S244 is used, add 2.5 ns to the timings.
3. The signal at 8284 or 8288 is for reference only.
4. The setup requirement, for asynchronous signal is only to guarantee recognition at the next CLK.
5. If BTHRDY = TRUE, READY must be set up 0.3 ns before the rising edge of T2.
6. If BTHRDY = TRUE, READY must be held 16.5 ns after the rising edge of T2.

A.C. CHARACTERISTICS FOR THE I2ICE™ SYSTEM 8088 PROBE (Continued)

Table 11. Maximum Complexity System Timing Responses

Min Mode Symbol	Parameter	5 MHz (8088)		8 MHz (8088-2)	
		Min ns	Max ns	Min ns	Max ns
TCLML(1)	Command Active Delay	10	35	10	35
TCLMH(1)	Command Inactive Delay	10	35	10	35
TRYHSH(2, 3, 4)	READY Active to Status Passive		37.5		37.5
TCHSV(4)	Status Active Delay	16.3	70.5	16.3	70.5 (60)
TCLSH(4)	Status Inactive Delay	10.5	42.5	10.5	42.5
TCLAV(4)	Address Valid Delay	17.5	72	17.5	72 (60)
TCLAX(5)	Address Hold Time	17.5		17.5	
TCLAZ(4)	Address Float Delay	13.6	61.5	13.6	61.5 (50)
TSVLH(1)	Status Valid to ALE High		15		15
TSVMCH(1)	Status Valid to MCE High		15		15
TCLLH(1)	CLK Low to ALE Valid		15		15
TCLMCH(1)	CLK Low to MCE High		15		15
TCHLL(1)	ALE inactive Delay		15		15
TCLMCL(1)	MCE Inactive Delay		15		15
TCLDV(4)	Data Valid Delay	17.5	70.5	17.5	70.5 (60)
TCHDX(5)	Data Hold Time	17.5		17.5	
TCVNV(1)	Control Active Delay	5	45	5	45
TCVNX(1)	Control Inactive Delay	10	45	10	45
TAZRL	Address Float to READ Active	−37.2(0)		−37.2(0)	
TCLRL(4)	$\overline{RD}$ Active Delay	15.9	110.5	15.9	110.5 (100)
TCLRH(4)	$\overline{RD}$ Inactive Delay	15.9	90.5	15.9	90.5 (80)
TRHAV	$\overline{RD}$ Inactive to Next Address	(Note 6)		(Note 6)	
TCHDTL(1)	Direction Control Active Delay		50		50
TCHDTH(1)	Direction Control Inactive Delay		30		30
TCLGL(4)	$\overline{GT}$ Active Delay	12.9	54.5	12.9	54.5 (50)
TCLGH(4)	$\overline{GT}$ Inactive Delay	14.9	65	14.9	65 (50)
TRLRH	$\overline{RD}$ Width	2TCLCL−82.5 (2TCLCL−75)		2TCLCL−82.5 (2TCLCL−50)	
TOLOH	Output Rise Time		20		20
TOHOL	Output Fall Time		12		12

Numbers followed by parentheses deviate from the 8088 chip specification; the 1985 *Microsystem Components Handbook* chip specification timing is given in the parentheses.

NOTES:
1. The signal at 8284 or 8288 is for reference only.
2. If BTHRDY = TRUE, READY must be set up 0.3 ns before the rising edge of T2.
3. For BTHRDY = TRUE, TRYHSH = TRYHCH + 47.
4. Timings are calculated with a 74F244 as the buffer for CLOCK or READY. If a 74S244 is used, add 2.5 ns to the timings.
5. Timings are calculated with a 74F244 as the buffer for CLOCK or READY. If a 74S244 is used, add 0.7 ns to the timings.
6. The address data lines are only floated during T4 when RD is active.

8086/8088 PROBE WAVEFORMS

MINIMUM MODE

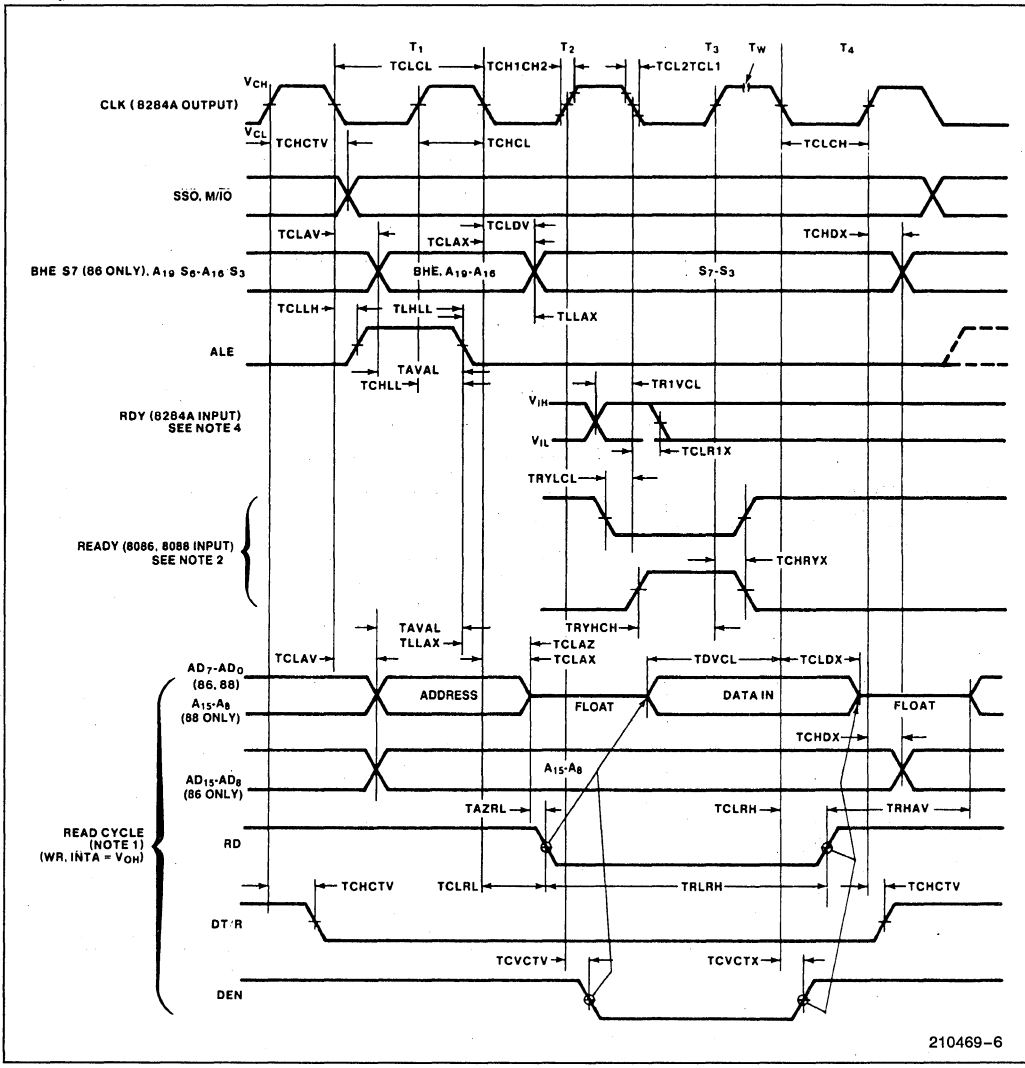
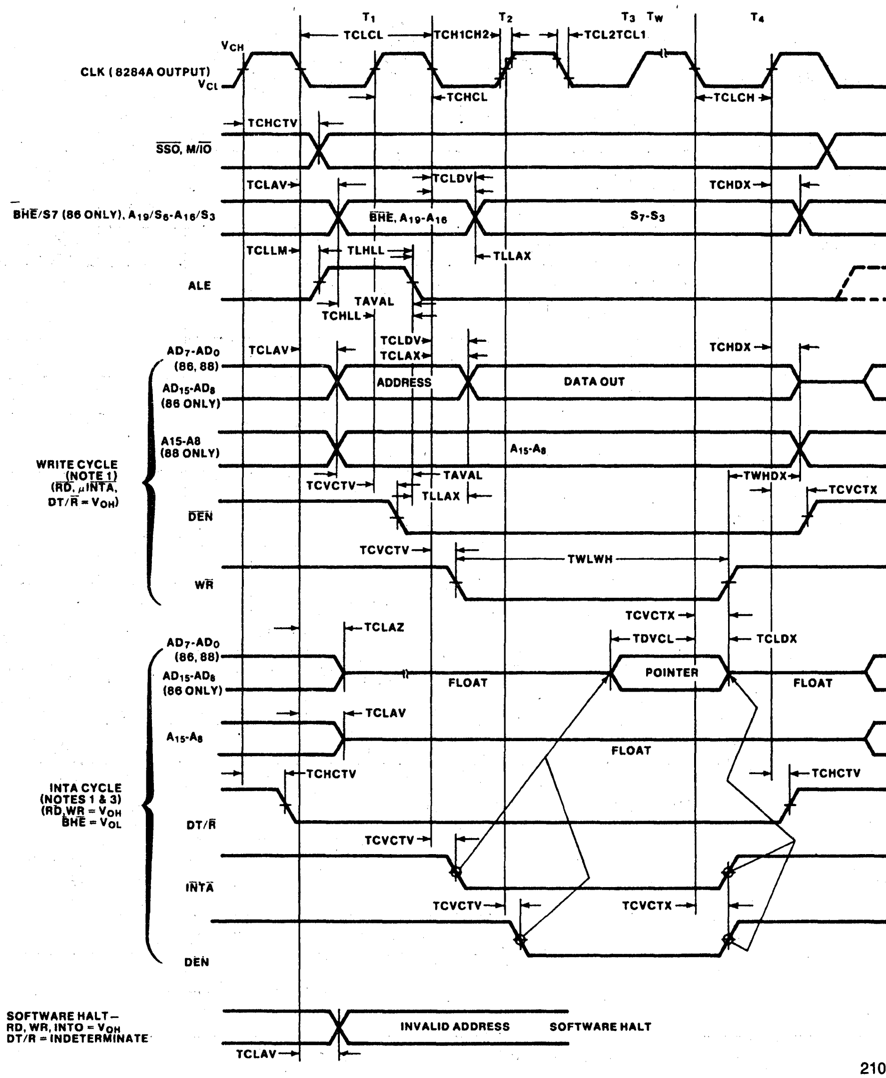


Figure 5. (Continued on next page)

8086/8088 PROBE WAVEFORMS (Continued)

MINIMUM MODE (Continued)



NOTES:

1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. READY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted. Timing shown is for BTHRDY = FALSE; see Figure 12 for BTHRDY = TRUE.
3. Two INTA cycles run back-to-back. The 8086 LOCAL ADDR/DATA BUS is floating during both INTA cycles. Control signals shown for second INTA cycle.
4. Signals at 8284A aer shown for reference only.

Figure 5. (Continued)

8086/8088 PROBE WAVEFORMS (Continued)

MAXIMUM MODE

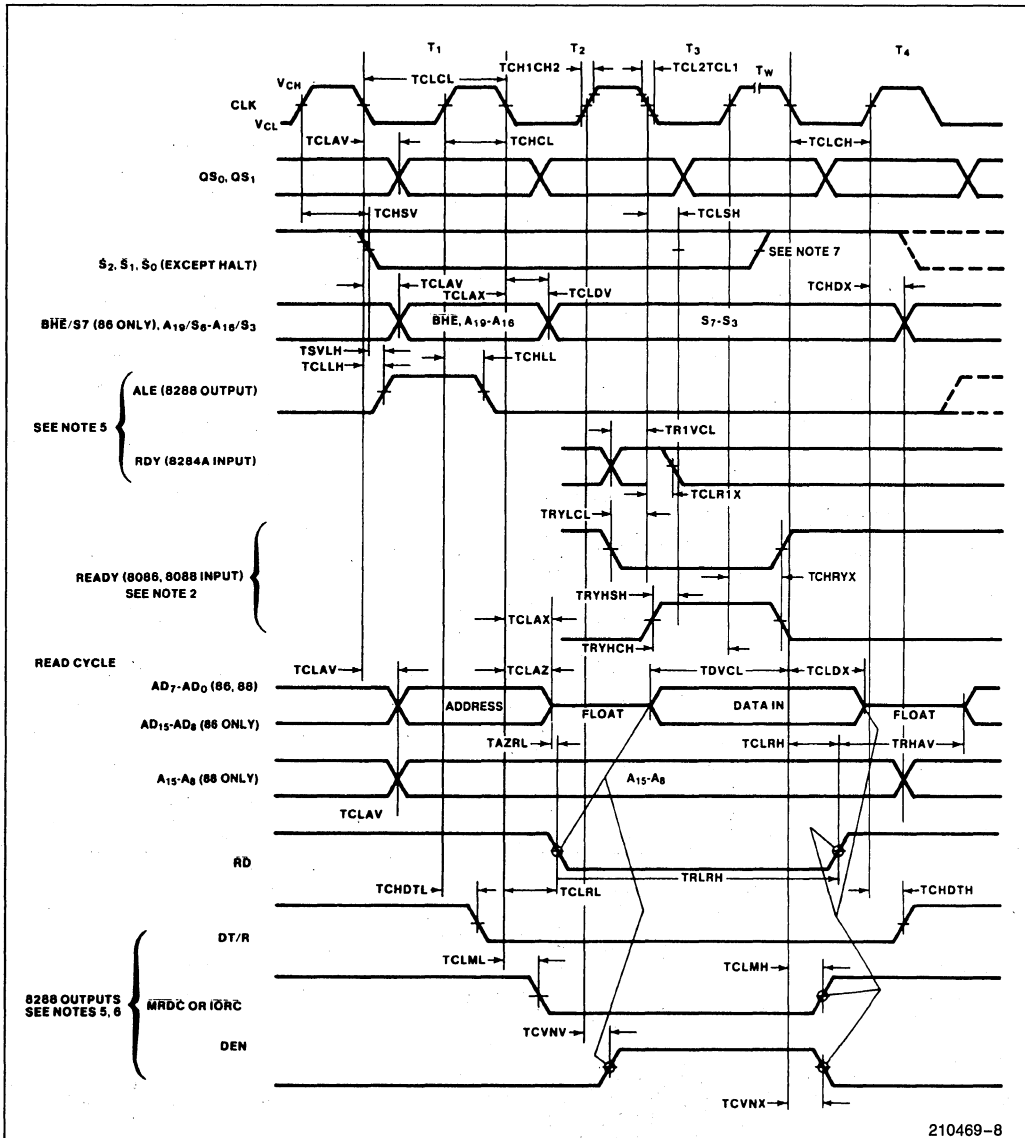
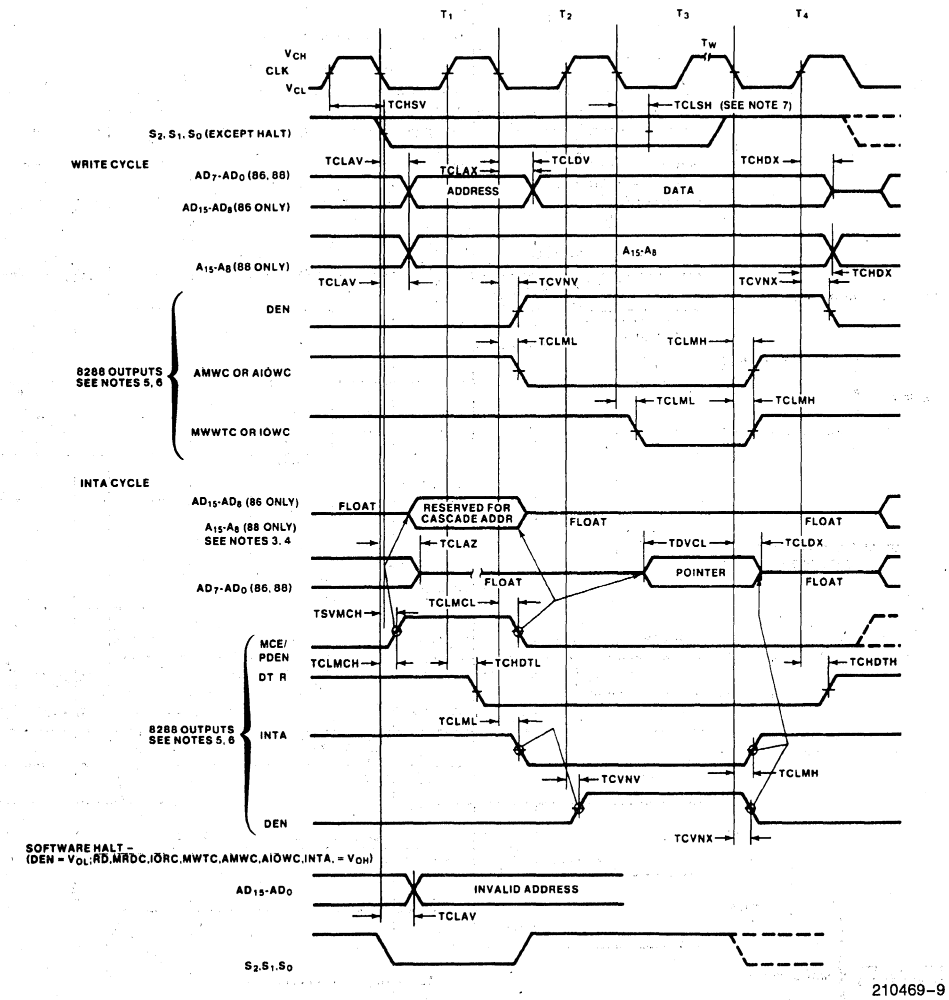


Figure 6. (Continued on next page)

8086/8088 PROBE WAVEFORMS (Continued)

MAXIMUM MODE (Continued)



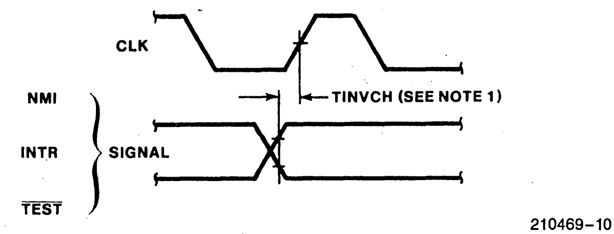
NOTES:

1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. READY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted. Timing shown is for BTHRDY = FALSE; see Figure 12 for BTHRDY = TRUE.
3. Cascade address is valid between first and second INTA cycle.
4. Two INTA cycles run back-to-back. The 8086 LOCAL ADDR/DATA BUS is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
5. Signals at 8284A and 8288 are shown for reference only.
6. The issuance of the 8288 command and control signals ($\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOC}$, $\overline{INTA}$, and $\overline{DEN}$) lags the active high 8288 CEN.
7. Status inactive in state just prior to T_4.

Figure 6. (Continued)

8086/8088 PROBE WAVEFORMS (Continued)

ASYNCHRONOUS SIGNAL RECOGNITION



NOTE:
1. Setup requirements for asynchronous signals only to guarantee recognition at next CLK.

Figure 7

BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)

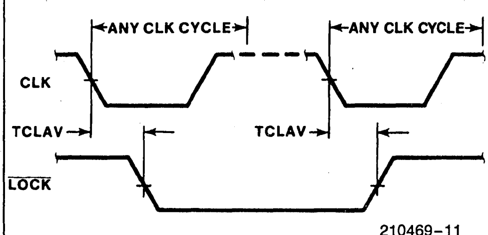


Figure 8

RESET TIMING

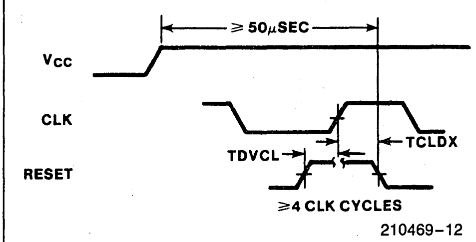
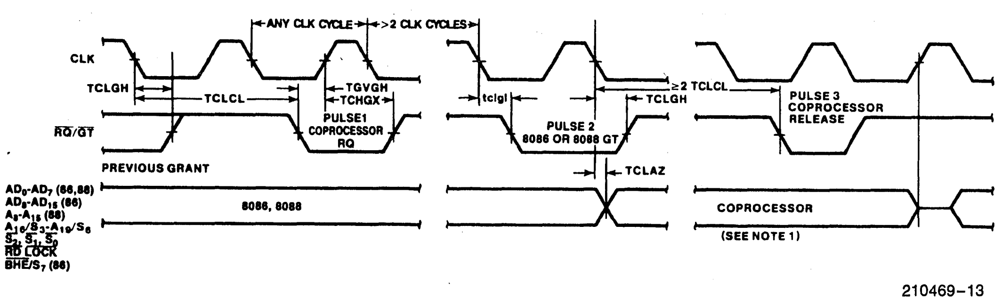


Figure 9

REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)



NOTE:
1. The coprocessor may not drive the buses outside the region shown without risking contention.

Figure 10

8086/8088 PROBE WAVEFORMS (Continued)

HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)

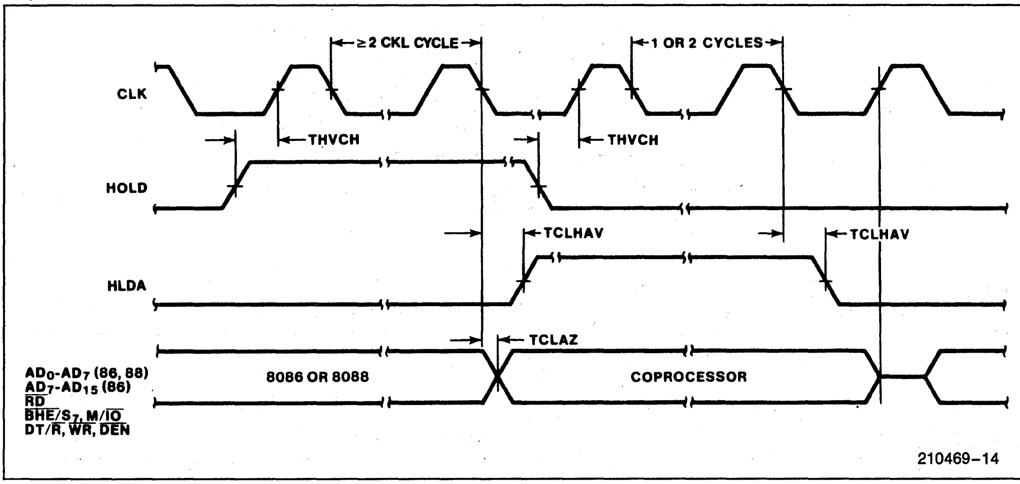


Figure 11

READY TIMING FOR BTHRDY = TRUE

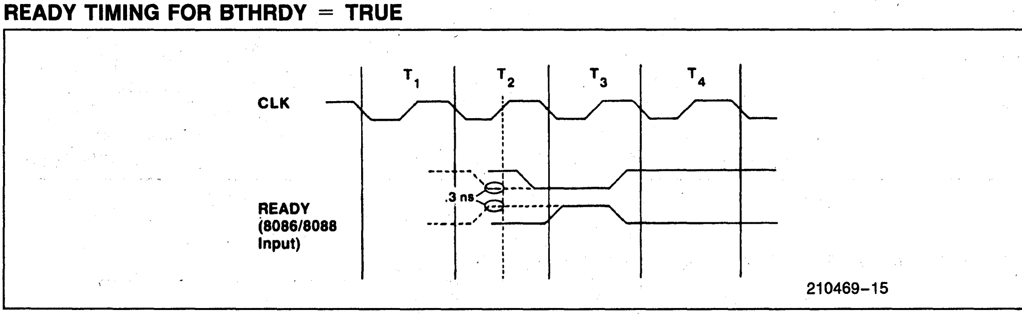


Figure 12

I²ICE™ SYSTEM 80186/80188 PROBE HIGHLIGHTS

- One megabyte addressing.
- Supports standard and queue status modes.
- Keyword access to the internal peripheral control block and the relocation register.

Table 12. I²ICE™ 80186/80188 User Interface—D.C. Characteristics

Pin Name	Input Voltage		Output Voltage		Input Current		Output Current	
	Max V_{IL} V	Min V_{IH} V	Max V_{OL} V	Min V_{OH} V	Max I_{IL} mA	Max I_{IH} mA	Max I_{OL} mA	Max I_{OH} mA
$\overline{X1}$	0.6	3.0			−0.0055	0.0055		
$\overline{RES}$	0.6	3.0			−0.0114	0.0082		
$\overline{TEST}$	0.6	2.2			−0.6	0.07		
TMRIN0, TMRIN1, DRQ0 DRQ1, NMI	0.6	2.2			−0.4	0.05		
HOLD	0.6	2.2			−1.6	0.04		
INT0, INT1	0.6	2.2			−0.21	0.03		
ARDY, SRDY	0.6	2.2			−2.0	0.07		
INT2/$\overline{INTA0}$, INT3/$\overline{INTA1}$	0.6	2.2	0.6	2.2	−0.21	0.03	2.0	−0.4
AD0–AD15	0.6	2.2	0.6	2.2	−0.45	0.1	64	−15
CLKOUT, A19/S6-A/16/S3, TMROUT0, TMROUT1, $\overline{BHE}$/S7, ALE/QS0, $\overline{WR}$/QS1, $\overline{RD}$/$\overline{QSMD}$, $\overline{LOCK}$, $\overline{S0}$, $\overline{S1}$, $\overline{S2}$, HLDA, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0-3}$, $\overline{PCS0-4}$, $\overline{PCS5}$/A1, $\overline{PCS6}$/A2, DT/$\overline{R}$, $\overline{DEN}$			0.6	2.2			64	−15
RESET			0.6	2.2			9.1	−15

NOTES:
1. Negative currents (−) are defined as currents flowing out of a terminal, and positive currents are defined as currents flowing into a terminal.
2. The 80186 and 80188 chip specifications indicate that the chips have an output drive capacity of I_{OH} = −400 μA and I_{OL} = 2.0 mA (2.5 mA for $\overline{S0}$–$\overline{S2}$); the chips' input and 3-state loading specification is ±10 μA. As can be seen from the table, the 80186/80188 probe has a greater output drive capacity than the 80186 or 80188 chip; it also presents greater input loading than the 80186 or 80188 chip (except for $\overline{X1}$ and the I_{IH} value for $\overline{RES}$).
3. The 80186/80188 probe does not draw any current from the user V_{CC}.

Capacitive Loading—80186/80188 Probe

- The 80186/80188 probe presents the user system with a maximum load of 80 pF (120 pF for ARDY, SRDY, and $\overline{TEST}$).

Coprocessor Operation—80186/80188 Probe

- The user can choose to have the coprocessor run only during emulation or all the time. If the coprocessor runs all the time, then during interrogation mode, the coprocessor may have as much as a one-microsecond delay.

AC CHARACTERISTICS FOR THE I2ICE™ SYSTEM 80186/80188 PROBE

All timings are measured at 1.5V unless otherwise noted. Tables 13 through 17 provide timing information for the 80186/80188 probe. Figures 13 through 15 define the timing symbols.

Table 13. Timing Requirements

Symbol	Parameter	8 MHz		Test Conditions
		Min ns	Max ns	
TDVCL	Data in Setup (A/D)	41.0 (20)		
TCLDX	Data in Hold (A/D)	−1.6		
TARYHCH	AREADY Active Setup Time	40.2 (20)		
TARYLCL	AREADY Inactive Setup Time	55.2 (35)		
TCHARYX	AREADY Hold Time	2.7		
TSYRCL	SREADY Transition Setup Time	45.2 (35)		
TCLSRY	SREADY Transition Hold Time	2.7		
THVCL	Hold Setup	42.5 (25)		
TINVCH	NMI Setup	76.0 (25)		NMI Only
TINVCH	INT0–INT3 Setup	37.0 (25)		INT0–INT3 Only
TINVCH	$\overline{TEST}$, TIMERIN Setup	46.0 (25)		All Others
TINVCL	DRQ0, DRQ1 Setup	41.0 (25)		

Numbers followed by parentheses deviate from the 80186/80188 chip specification; the 1984 *Microsystem Components Handbook* chip specification timing is given in the parentheses.

A.C. CHARACTERISTICS FOR THE I2ICE™ SYSTEM 80186/80188 PROBE
(Continued)

Table 14. Master Interface Timing Responses

Symbol	Parameter	8 MHz Min ns	8 MHz Max ns	Test Conditions
TCLAV	Address Valid Delay	−2.2 (5)	51.2 (44)	
TCLAX	Address Hold	−2.2 (10)		
TCLAZ	Address Float Delay	15.1	99.7 (35)	During HLDA Cycles Only
TCLAZ	Address Float Delay	14.8	52.0 (35)	During $\overline{RD}$ Cycles only
TCLAZ	Address Float Delay	−51.2 (TCLAX)	54.7 (35)	During $\overline{INTA}$ Cycles
TCHCZ	Command Lines Float Delay		151.7 (45)	
TCHCV	Command Lines Valid Delay (after Float)		66.2 (55)	
TLHLL	ALE Width	TCLCL−13.6 (TCLCL−35)		
TCHLH	ALE Active Delay		21.2	
TCHLL	ALE Inactive Delay		41.3 (35)	
TLLAX	Address Hold to ALE	TCHCL−34 (TCHCL − 25)		
TCLDV	Data Valid Delay	−2.2 (10)	43.2	
TCLDOX	Data Hold Time	−2.2 (10)		
TWHDX	Data Hold after $\overline{WR}$	TCLCL − 28.2		
TCVCTV	Control Active Delay(1)	−2.2 (5)	69.2	For $\overline{DEN}$
TCVCTV	Control Active Delay(1)	14.1	35.5	For $\overline{WR}$
TCVCTV	Control Active Delay(1)	−4.0 (5)	60.2	For $\overline{INTA}$
TCHCTV	Control Active Delay(2)	−2.2 (10)	62.2 (55)	
TCVCTX	Control Inactive Delay	−2.2 (5)	62.2 (55)	For $\overline{DEN}$
TCVCTX	Control Inactive Delay	14.1	35.5	For $\overline{WR}$
TCVCTX	Control Inactive Delay	−4.0 (10)	3.2	For $\overline{INTA}$
TCVDEX	$\overline{DEN}$ Inactive Delay (Non-Write Cycle)		69.2	
TAZRL	Address Float to $\overline{RD}$ Active	−35.6 (0)		

Numbers followed by parentheses deviate from the 80186/80186 chip specification; the 1984 *Microsystem Components Handbook* chip specification timing is given in the parentheses.

A.C. CHARACTERISTICS FOR THE I2ICE™ SYSTEM 80186/80188 PROBE
(Continued)

Table 14. Master Interface Timing Responses (Continued)

Symbol	Parameter	8 MHz		Test Conditions
		Min ns	Max ns	
TCLRL	RD Active Delay	14.1	35.5	
TCLRH	RD Inactive Delay	14.1	35.5	
TRHAV	RD Inactive to Address Active	TCLCL−37.2		
TCLHAV	HLDA Valid Delay	2.8 (10)	54.7 (50)	
TRLRH	RD Width	2TCLCL−19.3		
TWLWH	WR Width	2TCLCL		
TAVAL	Address Valid to ALE Low	TCLCH−26.6 (TCLCH−25)		
TCHSV	Status Active Delay	2.8 (10)	57.2 (55)	
TCLSH	Status Inactive Delay	2.8 (10)	62.2 (55)	
TCLTMV	Timer Output Delay		59.2	
TCLRO	Reset Delay		52.5	
TCHQSV	Queue Status Delay		34.2	

Numbers followed by parentheses deviate from the 80186/80186 chip specification; the 1984 *Microsystem Components Handbook* chip specification timing is given in the parentheses.

Table 15. Chip-Select Timing Responses

Symbol	Parameter	8 MHz	
		Min ns	Max ns
TCLCSV	Chip-Select Active Delay		65.2
TCXCSX	Chip-Select Hold from Command Inactive	17.8 (35)	
TCHCSX	Chip-Select Inactive Delay	−2.2 (5)	42.2 (35)

Numbers followed by parentheses deviate from the 80186/80188 chip specification; the 1984 *Microsystem Components Handbook* chip specification timing is given in the parentheses.

A.C. CHARACTERISTICS FOR THE I2ICE™ SYSTEM 80186/80188 PROBE
(Continued)

Table 16. CLKIN Requirements

Symbol	Parameter	8 MHz		Test Conditions
		Min ns	Max ns	
TCKIN	CLKIN Period	62.5	250.0	
TCKHL	CLKIN Fall Time		10.0	3.5V to 1.0V
TCKLH	CLKIN Rise Time		10.0	1.0V to 3.5V
TCLCK	CLKIN Low Time	25.0		
TCHCK	CLKIN High Time	25.0		

Table 17. CLKOUT Timing

Symbol	Parameter	8 MHz		Test Conditions
		Min ns	Max ns	
TCICO	CLKIN to CLKOUT Skew		97 (50)	
TCLCL	CLKOUT Period	125	500	
TCLCH	CLKOUT Low Time	1/2TCLCL−7.5		
TCHCL	CLKOUT High Time	1/2TCLCL−7.5		
TCH1CH2	CLKOUT Rise Time		15	1.0V to 3.5V
TCL2CL1	CLKOUT Fall Time		15	3.5V to 1.0V

Numbers followed by parentheses deviate from the 80186/80188 chip specification; the 1984 *Microsystem Components Handbook* chip specification timing is given in the parentheses.

80186/80188 PROBE WAVEFORMS

MAJOR CYCLE TIMING

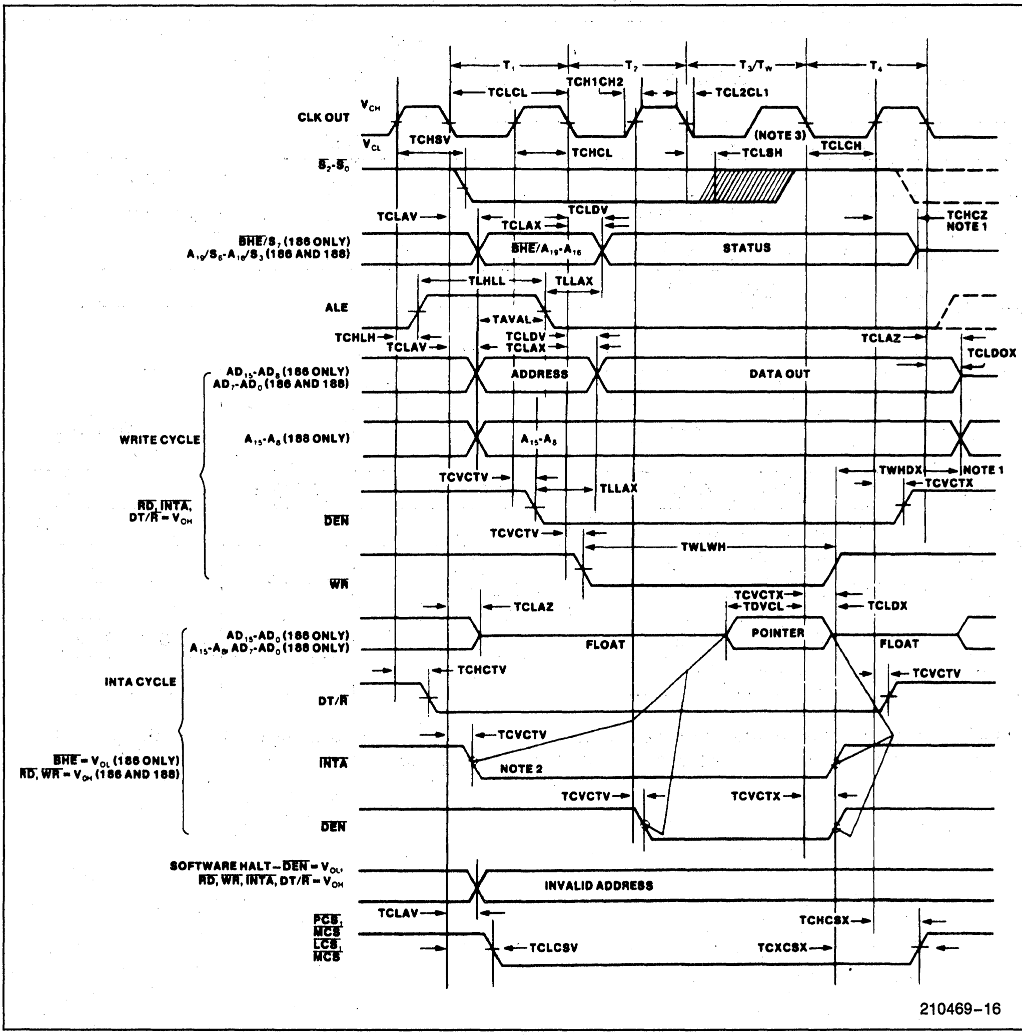
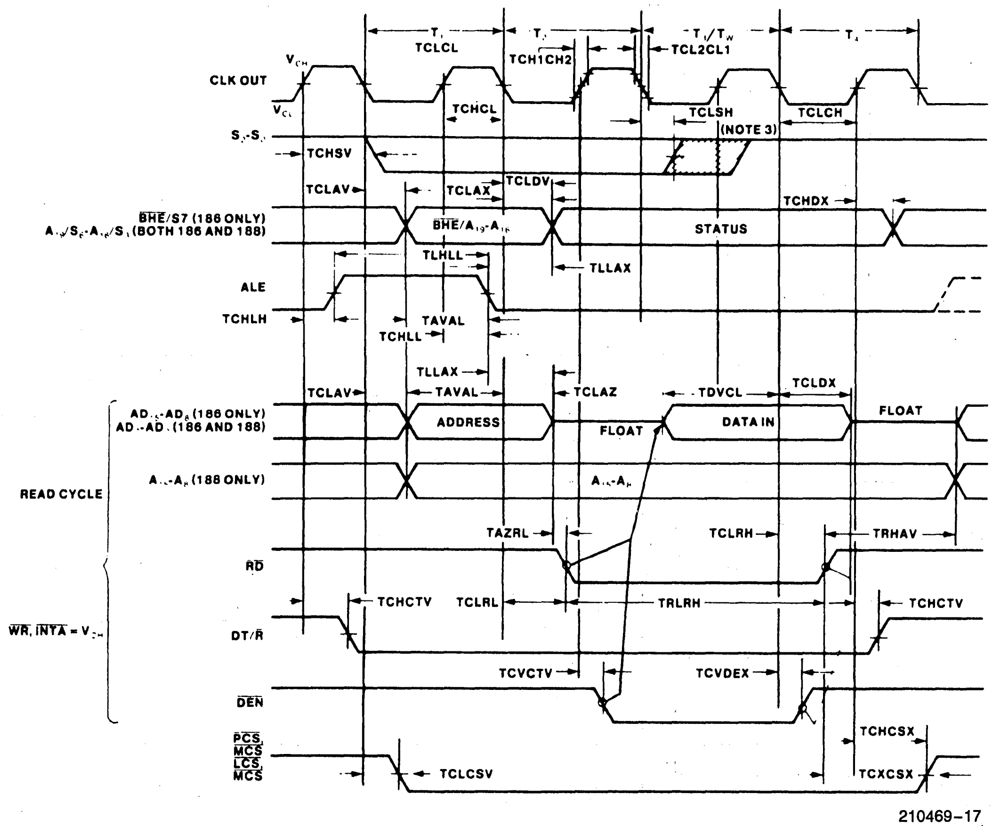


Figure 13 (Continued on next page)

80186/80188 PROBE WAVEFORMS (Continued)

MAJOR CYCLE TIMING (Continued)

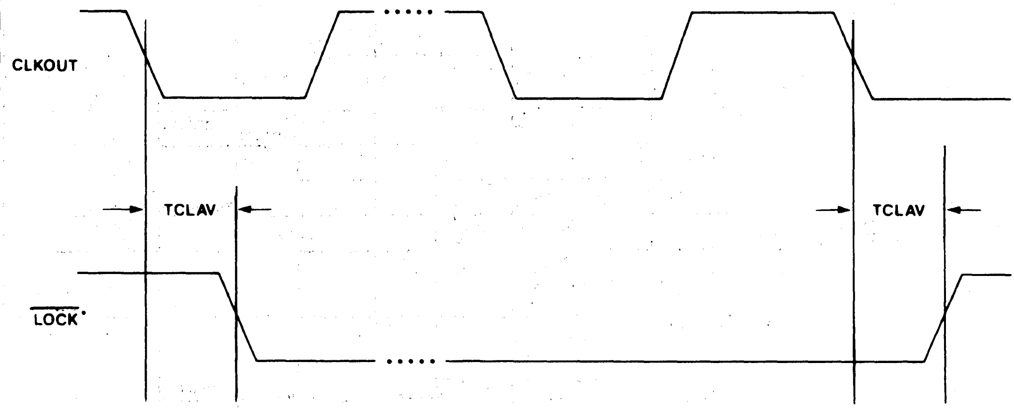


NOTES:
1. Following a Write cycle, the Local Bus is floated by the 80186/80188 only when the 80186/80188 enters a "Hold Acknowledge" state.
2. INTA occurs one clock later in RMX-mode.
3. Status inactive just prior to T.

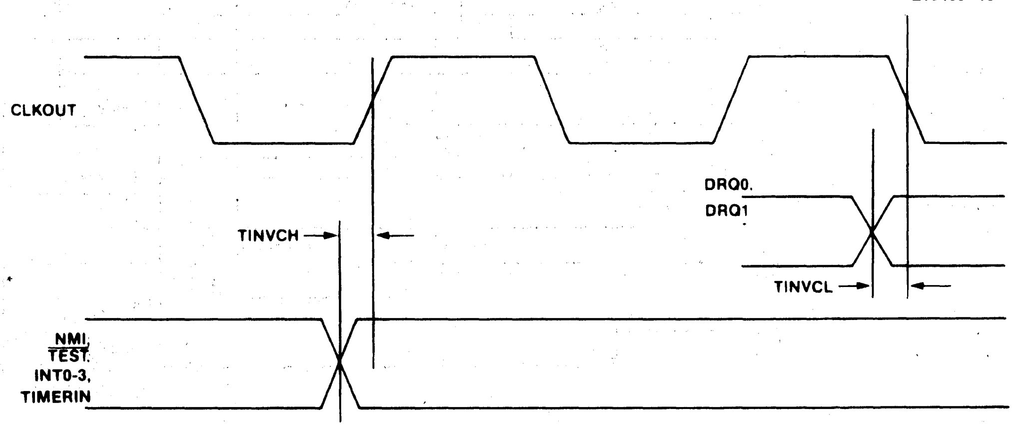
Figure 13 (Continued)

80186/80188 PROBE WAVEFORMS (Continued)

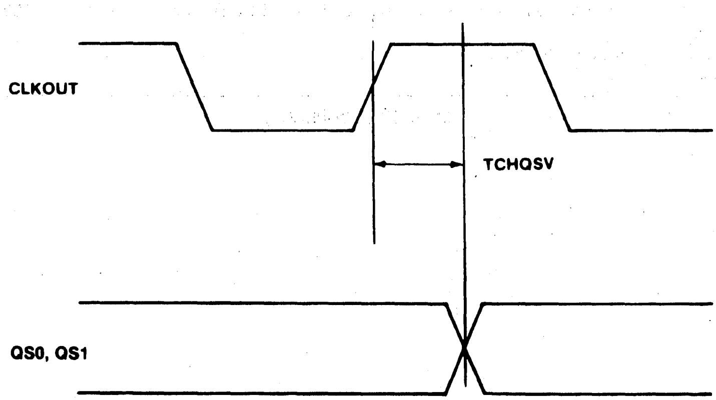
MAJOR CYCLE TIMING (Continued)



210469–18



210469–19



210469–20

Figure 13 (Continued)

80186/80188 PROBE WAVEFORMS (Continued)

HOLD-HLDA TIMING

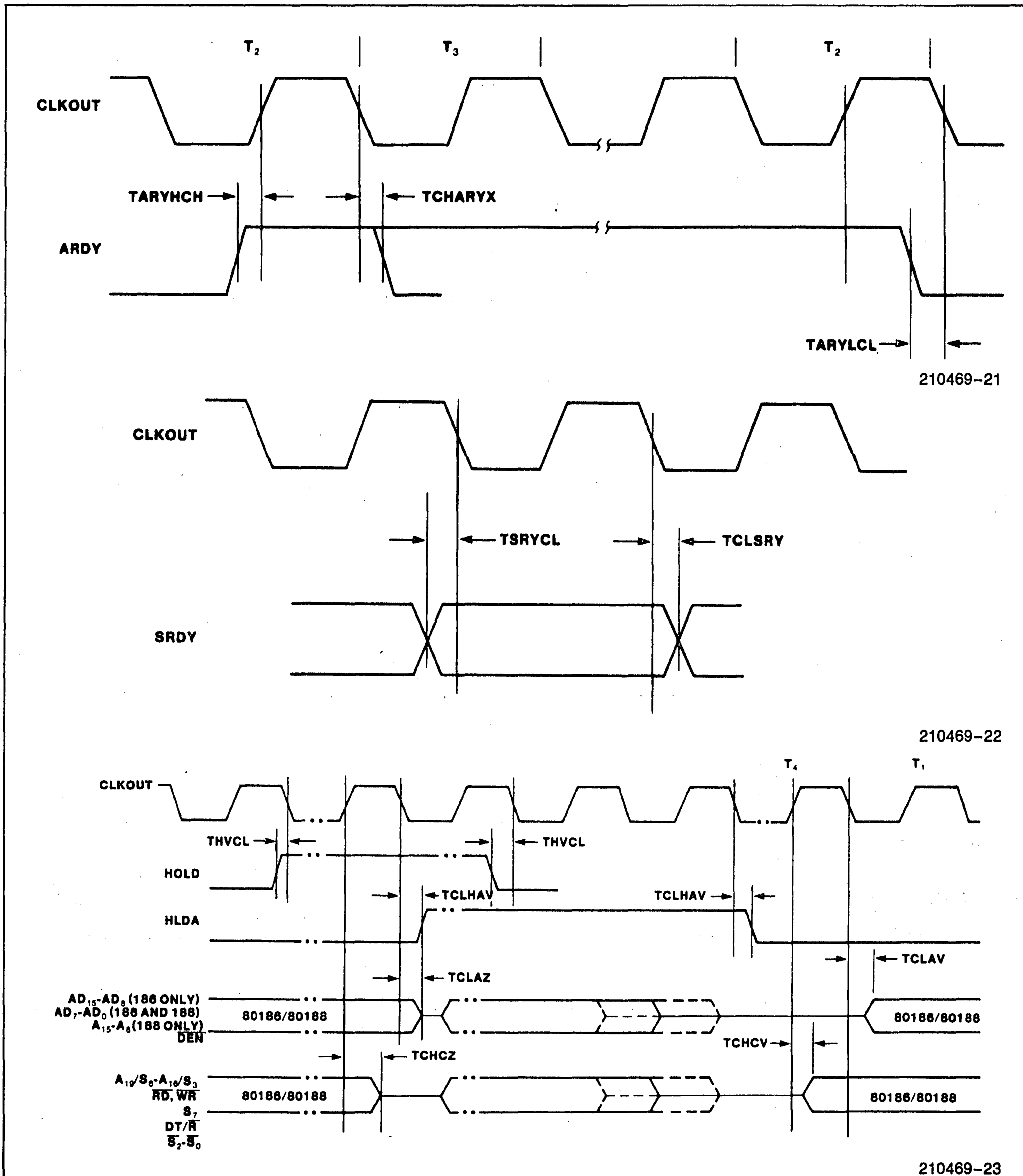


Figure 14

80186/80188 PROBE WAVEFORMS (Continued)

TIMER

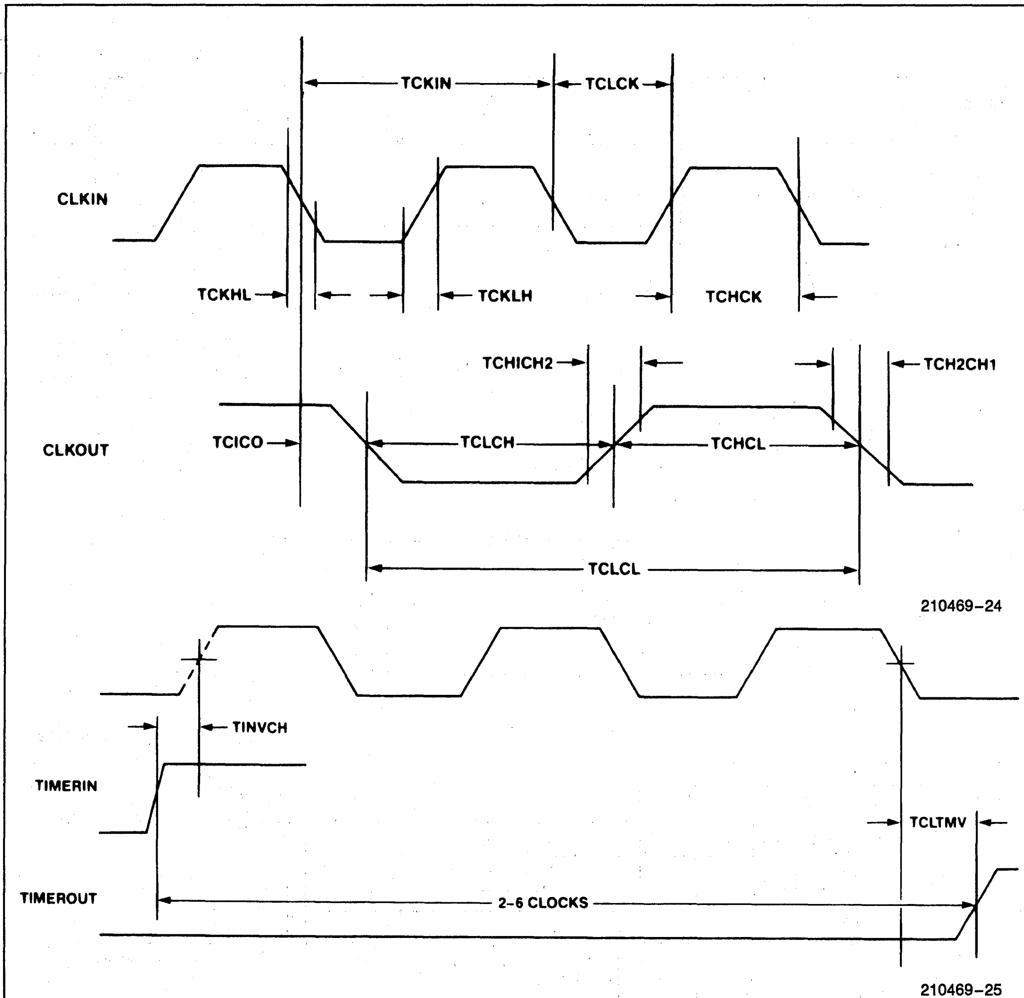


Figure 15

I^2ICE^{TM} SYSTEM 80286 PROBE HIGHLIGHTS

Both 6 MHz and 8 MHz probes are available. Each probe has the following features:

- Supports real and protected mode (software).
- Includes an object code loader for both 8086 and 80286 object files.
- Supports multiprocessing (with coprocessor and with the 80287 processor extension).
- Supports local descriptor tables (LDTs).
- Provides full 24-bit address mapping (with optional 16K granularity).
- Provides the capability to read/write normally invisible portions of segment and table registers.
- Supports multitasking.
- Does not slip on breakpoints.
- DMA (Hold/Hold Acknowledge) is supported in both emulation and interrogation modes.

Table 18. I^2ICE^{TM} 80286 User Interface—D.C. Characteristics: 6 MHz Probe/8 MHz Probe

Pin Name	Input Voltage		Output Voltage		Input Current		Output Current	
	Max V_{IL} V	Min V_{IH} V	Max V_{OL} V	Min V_{OH} V	Max I_{IL} mA	Max I_{IH} mA	Max I_{OL} mA	Max I_{OH} mA
A0–A23			0.6/0.6	2.2/2.2			12/12	−3/−3
D0–D15	0.6/0.6	2.2/2.2	0.6/0.6	2.2/2.2	−0.1/−0.7	0.02/0.07	12/20	−3/−3
$\overline{S0}$, $\overline{S1}$			0.75/0.75	2.2*/2.2*			64/64	−3.4/−3.4
M/$\overline{IO}$			0.75/0.75	2.2/2.2			64/64	−3.0/−3.0
$\overline{LOCK}$			0.75/0.75	2.2/2.2			64/64	−3.0/−3.0
COD/$\overline{INTA}$			0.75/0.75	2.2/2.2			64/64	−1/−3
$\overline{BHE}$			0.75/0.75	2.2/2.2			64/64	−1/−3
$\overline{ERROR}$	0.6/0.6	2.2/2.2			−2.15/−3.7	0.05/0.04		
$\overline{BUSY}$	0.6/0.6	2.2/2.2			−0.4/−0.7	0.05/0.02		
$\overline{PEACK}$			0.75/0.75	2.5/2.2			64/64	−1/−3
HLDA			0.75/0.75	2.5/2.2			64/64	−1/−3
HOLD	0.5/0.5	2.3/2.3			−0.4/−0.7	0.05/0.02		
PEREQ	0.6/0.6	2.2/2.2			−1.6/−0.7	0.02/0.02		
INTR	0.5/0.5	2.3/2.3			−1.6/−0.7	0.02/0.02		
NMI	0.6/0.6	2.2/2.2			−1.6/−0.7	0.02/0.02		
$\overline{CLK}$	0.6/0.6	2.2/2.2			−2.0/−0.7	0.07/0.02		
$\overline{READY}$	0.5/0.5	2.2/2.2			−3.6/−2.4	0.09/0.06		

NOTES:
*$\overline{S0}$ and $\overline{S1}$ have 5.1K pullup resistors.
1. DC characteristics are given in the form *m/n,* where *m* is the characteristic for the 6 MHz 80286 probe and *n* is the characteristic for the 8 MHz probe. Negative currents (−) are defined as currents flowing out of a terminal, and positive currents are defined as currents flowing into a terminal.
2. The 80286 chip specification indicates that the chip has an output drive capacity of $I_{OH} = -400\ \mu A$ and $I_{OL} = 2.0$ mA; the chip's input and 3-state loading specification is $\pm 10\ \mu A$. As can be seen from the above table, the 80286 probe has a greater output drive capacity and presents higher input loading than the 80286 chip.
3. The 80286 probe does not draw any current from the user V_{CC}.

Capacitive Loading—80286 Probe

- The 80286 probe presents the user system with a maximum capacitive load of 80 pF (100 pF for READY, HLDA, LOCK; 130 pF for HLD, ERROR, PEREQ, NMI RESET, INT, BUSY; and 160 pF for BHE).
- All 80286 probe outputs are capable of driving 0 pF while meeting all the probe's timing specifications. The 80286 probe will drive larger capacitive loads, but with possible performance degradation. Derate the timing specifications by 0.04 ns/pF corresponding to input capacitance of the user system.

A.C. CHARACTERISTICS FOR THE I2ICE™ 80286 SYSTEM PROBE

Table 19 provides timing information on the 80286 probe. Figures 16 through 19 define the timing symbols.

Table 19. Calculated Worst Case Timing Information

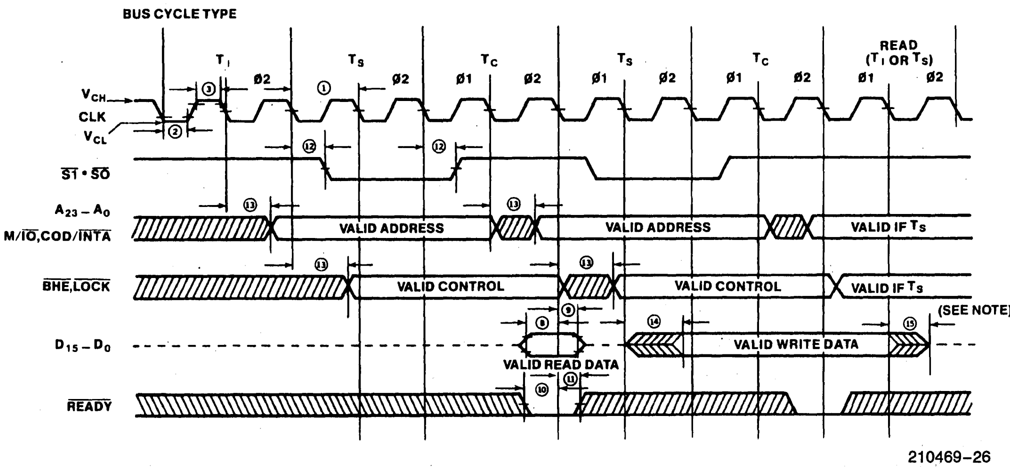
Symbol	Parameter	6 MHz Probe		8 MHz Probe	
		Min. ns	Max. ns	Min. ns	Max. ns
t1	System Clock Period	83	250	62	250
t2	System Clock Low Time	20	225	15	225
t3	System Clock High Time	25	230	225	235
t17	System Clock Rise Time		10		10
t18	System Clock Fall Time		10		10
t4	NMI, ITR, PEREQ, ERROR, BUSY Setup Time	27		20	
t4	HOLD Setup Time	40 (30)		28 (20)	
t5	NMI, INTR, PEREQ Hold Time	30		20	
t5	ERROR Hold Time	34 (30)		21 (20)	
t5	BUSY Hold Time	34 (30)		20	
t5	HOLD Hold Time	28		20	
t6	RESET Setup Time	12		28	
t7	RESET Hold Time	13 (5)		13 (5)	
t8	Read Data in Setup Time	20		11 (10)	
t9	Read Data in Hold Time	10 (8)		10 (8)	
t10	READY Setup Time	50		38	
t11	READY Hold Time	35		25	
t12	STATUS Valid Delay	10 (1)	55	1	44 (40)
t13	Address Valid Delay	10 (1)	80	1	65 (60)
t14	Write Data Valid Delay	9 (0)	65	0	59 (50)
t15	Address/STATUS/Data Float Delay (See Tables 20–23)	—	—	—	—
t15	Write Data Float Delay	10 (0)	34	0	50
t16	HLDA Valid Delay	9 (0)	80	0	60
t23	PEACK Valid Delay	10 (1)	80 (55)	1	48 (40)

Numbers followed by parentheses deviate from the 80286 chip specification; the 1985 *Microsystem Components Handbook* chip specification timing is given in the parentheses.

NOTE:
1. The symbols t1, t2, t3 . . . are references for the circled numbers on Figures 16, 17, 18, 19, and 24. For example to find t14 "Write Data Valid Delay" in Figure 16, look for a circled 14 on the figure.

80286 PROBE WAVEFORMS

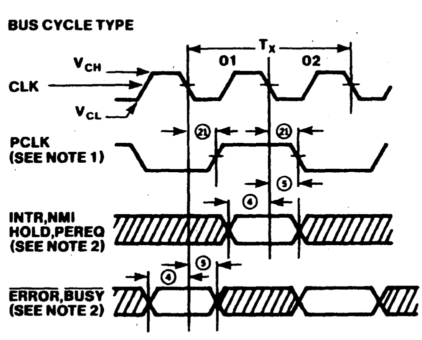
MAJOR CYCLE TIMING



NOTE:
Write data hold time can be increased by mapping memory to high-speed (HS) or optional high-speed (OHS) memory and using the WAITSTATE command to specify more waitstates than the number requested by the target system $\overline{READY}$. Write data hold time can be extended even further by mapping memory to MULTIBUS memory. Mapping I/O to the I2ICE system (using the ICE option with the MAPIO command) also causes write data hold time to increase for I/O write cycles.

Figure 16

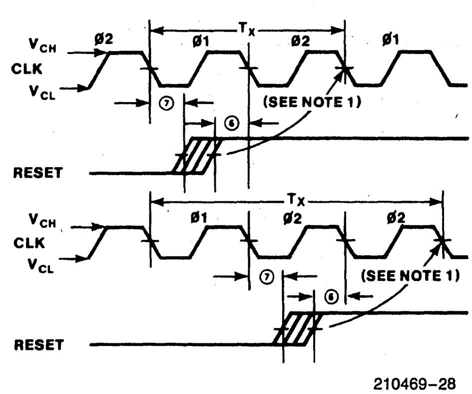
80286 ASYNCHRONOUS INPUT SIGNAL TIMING



NOTES:
1. PCLK indicates which processor cycle phase will occur on the next CLK. PCLK may not indicate the correct phase until the first bus cycle is performed.
2. These inputs are asynchronous. The setup and hold times shown assure recognition for testing purposes.

Figure 17

80286 RESET INPUT TIMING AND SUBSEQUENT PROCESSOR CYCLE PHASE

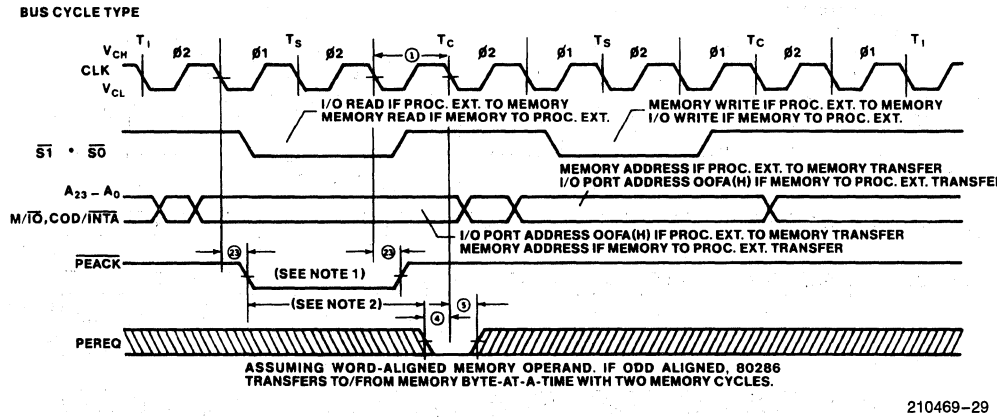


NOTE:
1. When RESET meets the setup time shown, the next CLK will start or repeat 02 of a processor cycle.

Figure 18

80286 PROBE WAVEFORMS (Continued)

80286 PEREQ/PEACK TIMING FOR ONE TRANSFER ONLY



NOTES:
1. PEACK always active during the first bus operation of a processor extension data operant transfer sequence. The first bus operation will be either a memory read at operand address or I/O at port address 00FA(H).
2. To prevent a second processor extension data operand transfer, the worst case maximum time (shown above) is: 3 × ① − ⑪ max. − 4 min. The actual, configuration-dependent, maximum time is: 3 × ① − ⑪ max. − ④ min + A × 2 × ①. A is the number of extra T_C states added to either the first or second bus operation of the processor extension data operand transfer sequence.

Figure 19

Interrupt Acknowledge Sequence Timing

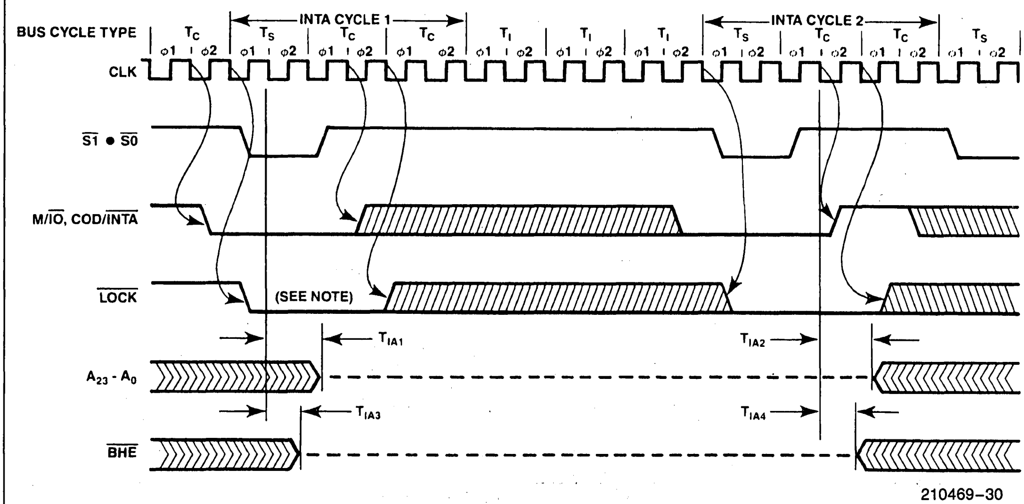
Figure 20 shows an interrupt acknowledge sequence for the 80286 probe. Table 20 provides timing information.

Table 20. Interrupt Acknowledge Timing

Symbol	Definition	6 MHz Probe		8 MHz Probe	
		Min. ns	Max. ns	Min. ns	Max. ns
T_{IA1}	Address Float Delay	14	59	19	60
T_{IA2}	Address Valid Delay	23	79	23	68
T_{IA3}	BHE Float Delay	14	56	18	51
T_{IA4}	BHE Valid Delay	18	68	17	51

80286 PROBE WAVEFORMS (Continued)

INTERRUPT ACKNOWLEDGE SEQUENCE TIMING



NOTE:
See pages 4–33 in the 1985 *Microsystem Components Handbook.*

Figure 20

80286 PROBE WAVEFORMS (Continued)

Reset Differences Between the 80286 and the I2ICE™ System 80286 Probe

There is a two-clock cycle delay that the I2ICE system 80286 probe adds to the RESET that it receives from the target system. This delay affects the initial 80286 pin state during reset as seen in the target system. A diagram showing the normal 80286 pin state during RESET can be found in the iAPS-286/10 data sheet. The effects of the two-clock delay and other emulator pin-state differences (as a function of target system RESET) are shown in Table 22. It should be noted that target system RESET has no effect if RSTEN is FALSE. The timing symbols used in Table 22, and Figures 21 and 22, are defined in Table 21.

Table 21. Timing Signal Definitions for Table 22 and Figures 21 and 22

Timing Signal	Definition
T_{R1}	User RESET Setup Time to User CLOCK Falling Edge.
T_{R2}	User RESET Hold Time after User CLOCK Falling Edge.
T_{R3}	ADDRESS Float Delay Due to RESET High. (1)
T_{R4}	ADDRESS Active after RESET Goes Low. (1)
T_{R5}	$\overline{BHE}$ Float Delay Due to RESET High. (1)
T_{R6}	$\overline{BHE}$ Active Delay after RESET Low. (1)
T_{R7}	M/$\overline{IO}$, $\overline{S0}$ and $\overline{S1}$ Float Delay after RESET High (1, 2)
T_{R8}	M/$\overline{IO}$, $\overline{S0}$ and $\overline{S1}$ Active Delay after RESET Low (1, 2)
T_{R9}	DATA Float Delay after RESET High. (1)
T_{R10}	$\overline{LOCK}$ High after RESET High. (1)
T_{R11}	COD/$\overline{INTA}$ Low after RESET High. (1)
T_{R12}	$\overline{PEACK}$ High after RESET High. (1)

NOTES:
1. RESET must meet setup and hold requirements T_{R1} and T_{R2}.
2. $\overline{S0}$ and $\overline{S1}$ are pulled up with 5.1K resistors on the emulator. The float delay in this case is the delay until status is no longer actively driven by the emulator. The active delay is the time until status is actively driven high.

Table 22. Emulator Pin State Differences Due to RESET

Symbol	Calculated Worst-Case				Number of CLOCK Edges After User RESET Goes High or Low
	6 MHz Probe		8 MHz Probe		
	Min. ns	Max. ns	Min. ns	Max. ns	
T_{R1}	12		23		Not Applicable
T_{R2}	13		13		Not Applicable
T_{R3}	31	97	35	85	2 (high)
T_{R4}	32	102	41	95	2 (low)
T_{R5}	32	109	35	79	2 (high)
T_{R6}	33	101	35	78	2 (low)
T_{R7}	26	83	32	72	2 (high)
T_{R8}	26	85	32	71	2 (low)—See Note 2 at Bottom of Table 21.
T_{R9}	19	62	28	66	2 (high)
T_{R10}	9	72	10	61	8 (high)
T_{R11}	10	76	10	61	9 (high)
T_{R12}	10	76	10	48	8 (high)

80286 PROBE WAVEFORMS (Continued)

Figure 21 and 22 show the RESET pin timing differences between the I2ICE 80286 probe and 80286 chip.

PIN TIMING DIFFERENCES DUE TO RESET FOR T_{R1} TO T_R

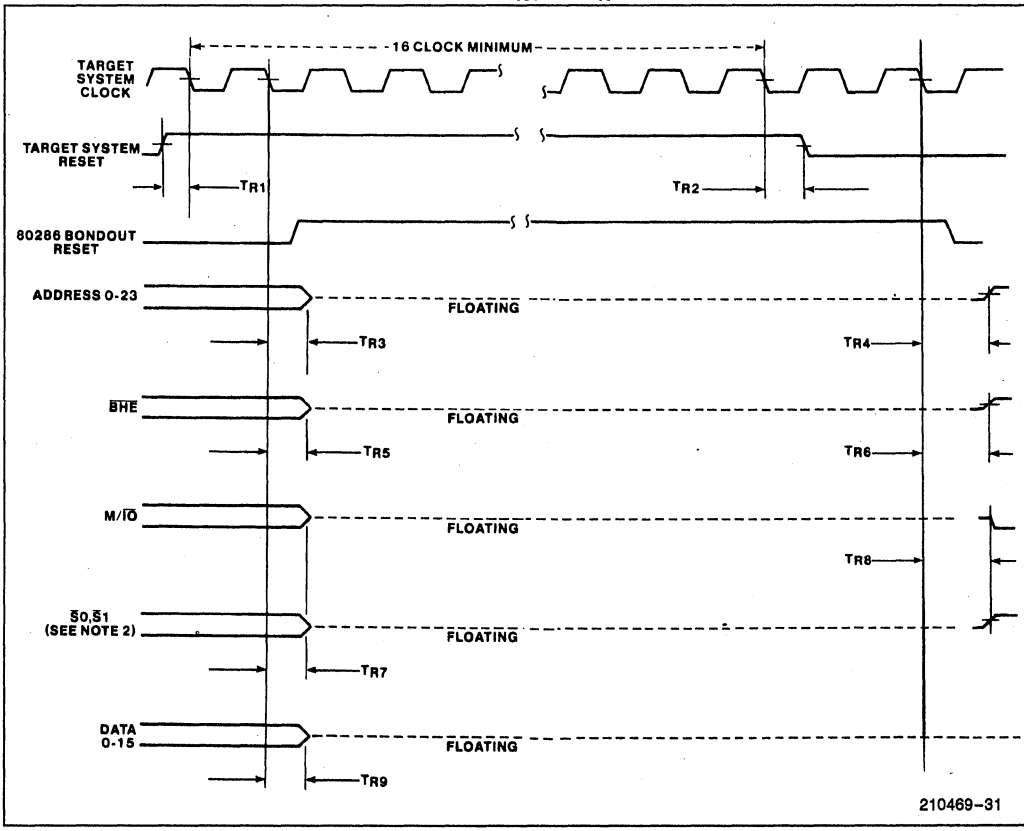


Figure 21

80286 PROBE WAVEFORMS (Continued)

PIN TIMING DIFFERENCES DUE TO RESET FOR T_{R10} TO T_{R12}

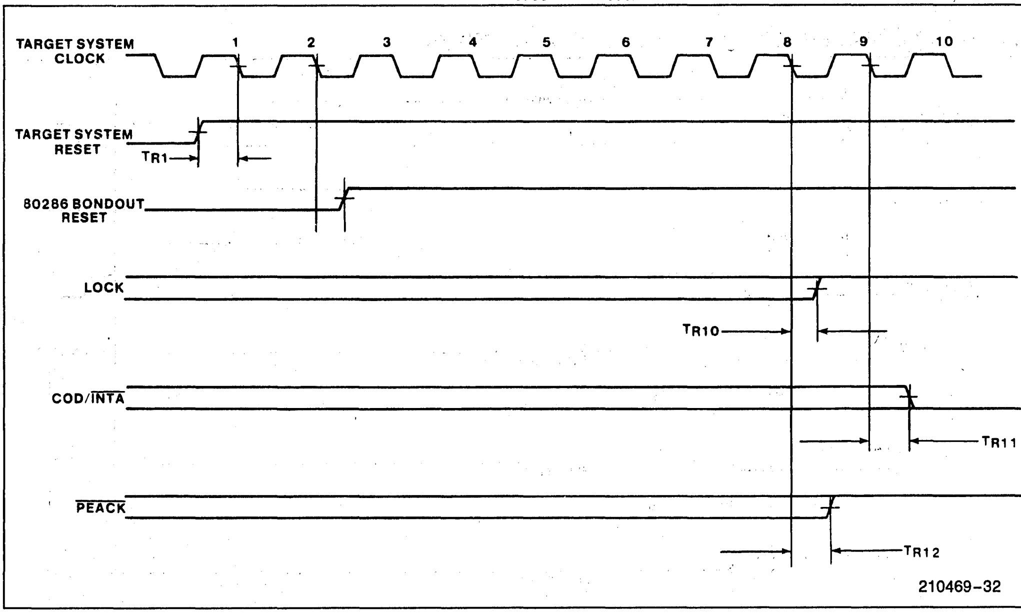


Figure 22

HOLD/HLDA Differences Between the 80286 and the I2ICE™ System 80286 Probe

There are differences in the pin timing parameters of the I2ICE 80286 probe and the 80286 as a function of HLDA. A diagram showing the pin timing while exiting and entering HOLD can be found in the iAPX-286/10 data sheet. There are two I2ICE pseudo-variables that control when a HOLD request will be honored. When COENAB is FALSE, HOLD requests from the target system are disabled. When COENAB is TRUE, the pseudo-variable CPMODE controls when HOLD is recognized. If CPMODE equals 1, HOLD will only be recognized when the probe is in emulation. If CPMODE is equal to 2, HOLD will always be recognized, even when the I2ICE system is in interrogation mode (not emulating). Table 24 gives the specification for the I2ICE 80286 pin timing as a function of HLDA. The timing signals used in Table 24, and Figures 23 and 24, are defined in Table 23.

Table 23. Timing Signal Definitions for Table 22 and Figures 23 and 24

Timing Signal	Definition
T_{H1}	$\overline{LOCK}$ Float Delay from HLDA High.(2)
T_{H2}	$\overline{LOCK}$ Active Delay from HLDA Low.(2)
T_{H3}	$\overline{BHE}$ Float Delay from HLDA High.
T_{H4}	$\overline{BHE}$ Active Delay from HLDA Low.
T_{H5}	M/$\overline{IO}$ Float Delay from HLDA High.
T_{H6}	M/$\overline{IO}$ Active Delay from HLDA Low.
T_{H7}	COD/$\overline{INTA}$ Float Delay from HLDA High.
T_{H8}	COD/$\overline{INTA}$ Active Delay from HLDA Low.
T_{H9}	ADDRESS 0–23 Float Delay from HLDA High.
T_{H10}	ADDRESS 0–23 Active Delay from HLDA Low.
T_{H11}	DATA 0–15 Float Delay from READY of Last Write Cycle before HLDA Goes HIgh. (80286 t15)
T_{H12}	DATA 0–15 Active Delay from HLDA Low. (80286 t14)
T_{H13}	$\overline{S0}$ and $\overline{S1}$ Float Delay from HLDA High.(1)
T_{H14}	$\overline{S0}$ and $\overline{S1}$ Active Delay from HLDA Low.(1)
T_{H15}	$\overline{PEACK}$ Float Delay from HLDA High.
T_{H16}	$\overline{PEACK}$ Active Delay from HLDA Low.
T_{H17}	HLDA High to Low Valid Delay.(3)
T_{H18}	HLDA Low to High Valid Delay.(3)

NOTES:
1. $\overline{S0}$ and $\overline{S1}$ are pulled up with 5.1K resistors on the emulator. The float delay in this case is the delay until status is no longer actively driven by the emulator. The active delay is the time until status is actively driven high.
2. The specified active delay indicates the time from the falling edge of target system clock until the I2ICE actively drives the signal. In some cases, the signal may not become valid until after the valid delay specified for normal (no HLDA) bus cycles. One such case is $\overline{LOCK}$.
3. All float delays and active delays (except T_{H11} and T_{H12}) are due to a combinational delay from HLDA.

Table 24. Pin Timing Differences Due to HOLD

Symbol	Calculated Worst-Case			
	6 MHz Probe		8 MHz Probe	
	Min ns	Max ns	Min ns	Max ns
T_{H1}	19	112	20	81
T_{H2}	19	112	19	78
T_{H3}	21	120	22	85
T_{H4}	21	115	21	82
T_{H5}	18	113	17	78
T_{H6}	20	113	17	75
T_{H7}	17	106	17	75
T_{H8}	19	106	16	72
T_{H9}	21	119	22	91
T_{H10}	22	127	21	82
T_{H11}	*	*	*	*
T_{H12}	*	*	*	*
T_{H13}	18	113	17	78
T_{H14}	19	113	17	75
T_{H15}	17	106	17	75
T_{H16}	17	105	16	72
T_{H17}	9	80	0	60
T_{H18}	9	80	0	60

*See Figures 23 and 24.

80286 PROBE WAVEFORMS (Continued)

ENTERING AND EXITING HOLD

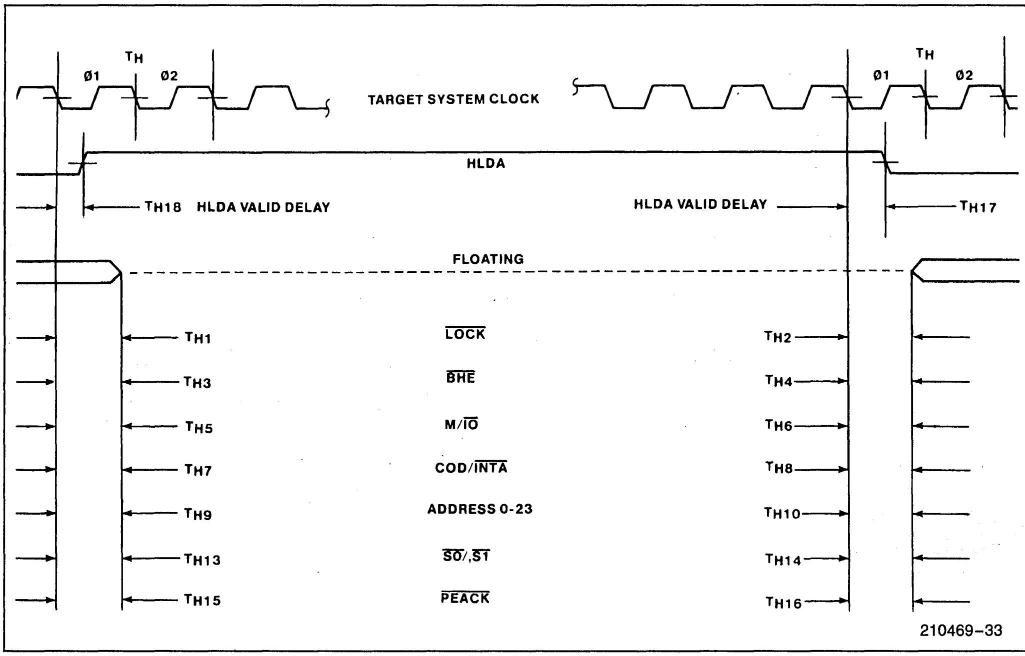
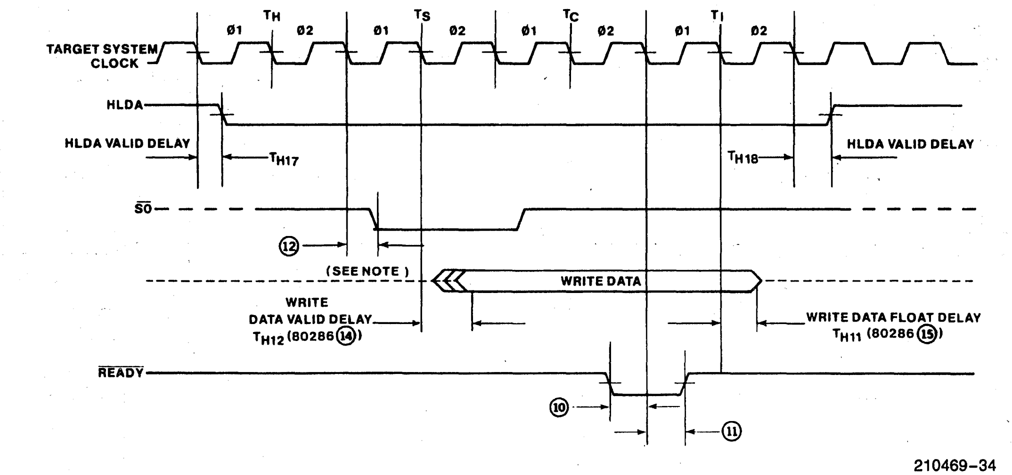


Figure 23

80286 PROBE WAVEFORMS (Continued)

EXITING AND ENTERING HOLD (Continued)



NOTE:
1. The data bus will remain 3-state OFF if a read cycle is performed.

Figure 24

Available Documentation

122143	*AEDIT™ Text Editor User's Guide*
121790	*PSCOPE 86 High-Level Program Debugger User's Guide*
166298	*I^2ICE^{TM} System User's Guide*
166302	*I^2ICE^{TM} System Reference Manual*
166305	Installation Supplement for *I^2ICE^{TM} System User's Guide* for Intel hosts
166306	Installation Supplement for *I^2ICE^{TM} System User's Guide* for IBM PC hosts
163256	*iLTA User's Guide*
163257	*iLTA Reference Manual*
163258	*iLTA Learner's Guide*
210350	*PSCOPE 86 data sheet*
230839	*iLTA data sheet*

ORDERING INFORMATION

Order Code	Description: Kits for Series III Host
III010KITB	I^2ICE system 8086/8088 support kit for Series III host. Includes III086A902B (8086/8088 probe and software), III515 (instrumentation chassis and emulation base module), and III520B952B (host interface module and host software).
III110KITB	I^2ICE system 80186/80188 support kit for Series III host. Includes III186A912B (80186/80188 probe and software) III515 (instrumentation chassis and emulation base module), and III520B952B (host interface module and host software).
III210KITB	I^2ICE system 6 MHz 80286 support kit for Series III host. Includes III286A922B (6 MHz 80286 probe and software), III515 (instrumentation chassis and emulation base module), and III520B952B (host interface module and host software).

Order Code	Description: Kits for Series III Host (Continued)
IIIOLAKITB	I2ICE system iLTA-OHS support kit for Series III host. Includes III707 (OHS memory board), III515 (instrumentation chassis and emulation base module), III810A982B (logic timing analyzer and iLTA host software), and III520B952B (host interface module and host software).
III811KITB	Series III iLTA kit, includes III810A982B (iLTA hardware and software) and III820 (IOC board)

Order Code	Description: Probes and Interface Module with Required Software for Series III Host
III086A902B	I2ICE system 8086/8088 emulation personality module (probe) and probe software (8-in. single-density and double-density disks).
III186A912B	I2ICE system 80186/80188 emulation personality module (probe) and probe software (8-in. single-density and double-density disks).
III286A922B	I2ICE system 6 MHz 80286 emulation personality module (probe) and probe software (8-in. single-density and double-density disks).
III286B922B	I2ICE system 8 Mhz 80286 emulation personality module (probe) and probe software (8-in. single-density and double-density disks).
III520B952B	Series III host interface module; includes host interface board, cables, and I2ICE system host software (8-in. single-density and double-density disks).

Order Code	Description: Kits for Series IV Host
III010KITC	I2ICE system 8086/8088 support kit for Series IV host. Includes III186A903C (8086/8088 probe and software), III515 (instrumentation chassis and emulation base module), and III520B953C (host interface module and host software).
III110KITC	I2ICE system 80186/80188 support kit for Series IV host. Includes III186A913C (80186/80188 probe and software), III515 (instrumentation chassis and emulation base module), and III520B953C (host interface module and host software).
III210KITC	I2ICE system 6 MHz 80286 support kit for Series IV host. Includes III286A923C (6 MHz 80286 probe and software), III515 (instrumentation chassis and emulation base module), and III520B953C (host interface module and host software).
IIIOLAKITC	I2ICE system iLTA-OHS software kit for Series IV host. Includes III707 (OHS memory board), III515 (instrumentation chassis and emulation base module), and III810A983C (logic timing analyzer and iLTA host software), and III520B953C (host interface module and host software).

Order Code	Description: Probes and Interface Module with Required Software for Series IV Host
III086A903C	I2ICE system 8086/8088 emulation personality module (probe) and probe software (5¼-in. double-density disk).
III186A913C	I2ICE system 80186/80188 emulation personality module (probe) and probe software (5¼-in. double-density disk).
III286A923C	I2ICE system 6 MHz 80286 emulation personality module (probe) and probe software (5¼-in. double-density disk).

Order Code	Description: Probes and Interface Module with Required Software for Series IV Host (Continued)
III286B923C	I2ICE system 8 MHz 80286 emulation personality module (probe) and probe software (5¼-in. double-density disk).
III520B953C	Series IV host interface module; includes the host interface board, cables, and I2ICE system host software (5¼-in. double-density disks).

Order Code	Description: Kits for IBM PC Host
III010KITD	I2ICE system 8086/8088 support kit for IBM PC host. Includes III086A904D (8086/8088 probe and software), III515 (instrumentation chassis and emulation base module), and III520AT954D (host interface module and host software).
III110KITD	I2ICE system 80186/80188 support kit for IBM PC host. Includes III186A914D (80186/80188 probe and software), III515 (instrumentation chassis and emulation base module), and III520AT954D (host interface module and host software).
III210KITD	I2ICE system 6 MHz 80286 support kit for IBM PC host. Includes III286A924D (6 MHz 80286 probe and software), III515 (instrumentation chassis and emulation base module), and III520AT954D (host interface module and host software).

Order Code	Description: Probes and Interface Module with Required Software for IBM PC Host
III086A904D	I2ICE system 8086/8088 emulation personality module (probe) and probe software for PC-DOS (5¼-in. double-density disks).
III186A914D	I2ICE system 80186/80188 emulation personality module (probe) and probe software for PC-DOS (5¼-in. double-density disk).
III286A924D	I2ICE system 6 MHz 80286 emulation personality module (probe) and probe software for PC-DOS (5¼-in. double-density disk).
III286A924D	I2ICE system 8 MHz 80286 emulation personality module (probe) and probe software for PC-DOS (5¼-in. double-density disk).
III520AT954D	IBM PC host interface module; includes the host interface board, cable, and I2ICE system host software for PC-DOS (5¼-in. double-density disks).

Order Code	Description: I2ICE System Instrumentation Chassis and Optional High Speed Memory for Series III and IV and IBM PC Hosts
III515	I2ICE system instrumentation chassis and emulation base module; includes the instrumentation chassis, emulation base module with memory map I/O board, break/trace board, emulator base, and emulation clips assembly.
III707	I2ICE system optional high speed (OHS) memory board, 128K bytes.

Order Code	Description: iLTA Logic Timing Analyzer, Cables, and Accessories
III810A982B	I2ICE system logic timing analyzer and software for operation with a Series III host (8-in. single-density and double-density disks).
III810A983C	I2ICE system logic timing analyzer and software for operation with a Series IV host (5¼-in. double-density disks).

Order Code	Description: iLTA Logic Timing Analyzer, Cables, and Accessories (Continued)
III530	Cable, host-to-chassis, 3 m (10 ft.) [only for use with Model 800 hosts].
III531*	Cable, host-to-chassis, 12.8 m (42 ft.) [only for use with Model 800 hosts].
III531A*	Cable, host-to-chassis (for Series III and Series IV hosts); 12.2 m (40 ft).
III532A	Cable set, inter-chassis; 0.6 m (2 ft).
III533A*	Cable set, inter-chassis; 3 m (10 ft).
III621	I²ICE system emulator clips assembly.
III815	I²ICE system micro hook set (40).
III820	IOC board upgrade for iLTA on Series III development system.

*Do not use III531 or III531A with III533A because total cable length must be less than 15.2 m (50 ft.)

Order Code	Description: Extra I²ICE System Software
902B	I²ICE system 8086/8088 probe software for Series III (8-in. single-density and double-density disks).
903C	I²ICE system 8086/8088 probe software for Series IV (5¼-in. double-density disk).
904D	I²ICE system 8086/8088 probe software for PC-DOS (5¼-in. double-density disk).
912B	I²ICE system 80186/80188 probe software for Series III (8-in. single-density and double-density disks).
913C	I²ICE system 80186/80188 probe software for Series IV (5¼-in. double-density disk).
914D	I²ICE system 80186/80188 probe software for PC-DOS (5¼-in. double-density disk).
922B	I²ICE system 80286 probe software for Series III (8-in. single-density and double-density disks).
923C	I²ICE system 80286 probe software for Series IV (5¼-in. double-density disk).
924D	I²ICE system 80286 probe software for PC-DOS (5¼-in. double-density disk).
952B	I²ICE system host software for Series III (8-in. single-density and double-density disks).
953C	I²ICE system host software for Series IV (5¼-in. double-density disks).
954D	I²ICE system host software for PC-DOS (5¼-in. double-density disks).
982B	I²ICE system iLTA software for Series III (8-in. single-density and double-density disks).
983C	I²ICE system iLTA software for Series IV (5¼-in. double-density disks).

Order Code	Description: PSCOPE on IBM PC-DOS
iPSC86DOS	PSCOPE software that runs on IBM PC-DOS.