Most Significant Bits

C&T Bails Out of Multiprocessor Chip Set Biz

Chips and Technologies is withdrawing its M/PAX multiprocessor chip set from the market, following almost two years of largely unsuccessful attempts to convince system makers to use it. (See µPR 2/21/90, p.1 for details on M/PAX.) C&T is offering the technology for sale, hoping that it will be more attractive to a computer company as the basis for a proprietary system design than it was as a merchant-market chip set.

C&T is not the first company to run into difficulty trying to sell chip sets for multiprocessor PCs. S3, a C&T spin-off, announced plans for a comprehensive multiprocessor chip set in May 1990 (see µPR 5/18/90 p. 1), a few months after C&T's announcement, but S3 never shipped the product. A combination of lackluster market interest in multiprocessor PCs and development difficulties caused S3 to scrap the entire product line a year later.

While C&T did succeed in shipping a working multiprocessor chip set, it encountered the same market problem S3 faced: there just isn't much demand for multiprocessor PCs. A few companies have successfully sold them as multiuser UNIX systems, but this is a tiny market for a company like C&T. Compaq's two-processor-capable Systempro is probably the most successful multiprocessor PC yet, but the vast majority of Systempros are sold with only one processor installed.

The root problem is the lack of software that can take advantage of a multiprocessor system. Multiple processors are easy to exploit in a server or a multiuser system, which always has numerous tasks running. For desktop, single-user systems, however, there isn't any software in widespread use that can make effective use of more than one processor. This may change with multithreaded, multitasking operating systems such as Windows NT, but the single-user, multiprocessor system market will grow very slowly.

C&T's withdrawal leaves the market to Corollary, a small Irvine-based company that has pioneered multiprocessor PC technology. (Intel also has announced a cache controller for multiprocessor 486 systems, but it has never introduced the promised multiprocessor interrupt controller and does not provide a complete system design.) Corollary has licensed a PAL-based system design to several vendors, and it is now developing a new multiprocessor system design based on two custom chips (see µPR 8/21/91, p. 1). The multiprocessor PC market today makes a much better business opportunity for a small, technology-oriented company such as Corollary than it does for a chip-set maker like C&T. From the system makers' point of view, Corollary is a better supplier because it is committed to MP systems.

IIT Vision Processor in AT&T Videophone

Integrated Information Technology (IIT), a small Santa Clara-based chip maker best known for its Intel-compatible math coprocessors, has scored a major design win for its Vision Processor (VP) chip (see µPR 10/30/91, p. 1) in AT&T's new $1500 Videophone 2500. The video compression circuitry in the AT&T phone was developed by Compression Labs of San Jose, which codeveloped the VP chip with IIT. AT&T added its own audio and modem circuits to complete the Videophone design. In addition, Compression Labs has introduced a video conferencing add-in board for the Macintosh, which is also based on IIT's VP chip.

The Videophone 2500 brings the "picturephone" down to a far lower price than ever before, but it still isn't clear that it will be a volume success. The tiny 3.3-inch-square LCD screen is too small for business teleconferencing applications, and home picturephones have one key problem: most people don't want to be seen when they're on the phone. (See "Who Needs Multimedia," µPR 6/12/91, p. 13, for more on this topic.)

ULSI Allowed to Continue Shipments

Last month, an Oregon judge granted Intel a preliminary injunction, based on claims of patent infringement, that could have prevented ULSI Technology from shipping its 387-compatible math coprocessor. That injunction has now been stayed pending appeal, allowing ULSI to continue shipping its chips.

The week after the Oregon judge granted the preliminary injunction, a San Jose superior court judge refused to grant an injunction in a separate trade-secret case brought by Intel against ULSI. At issue in this case is whether the designers at ULSI used information from confidential Intel documents that belonged to one of ULSI's early employees, who had previously worked at Intel. Of particular concern is an Intel "T-spec" (target specification) that was found in the possession of a former IIT employee. While accepting Intel's argument that portions of IIT's design appeared to be influenced by the T-spec, he questioned whether the information used from the T-spec is trade-secret information.

ULSI president George Hwang asserts that Intel's lawsuits are without merit and are intended to drain ULSI's resources while setting an example for other prospective competitors. The message Intel wants to get across, according to Hwang, is that if you compete with Intel, you'll end up in court.

Moto Ships NEURON Chips, Invests in Echelon

Motorola has announced general sampling of Echelon's "NEURON" chip, which Motorola designates the MC143150. The chip, which serves as a node in Eche-

lon's distributed control scheme, was designed by Echelon and licensed to Motorola and Toshiba. It implements Echelon's LONTALK protocol and can interface to a variety of input and output devices (see µPR 12/12/90 p. 1). The LON system is supported by the LONBUILDER development system, which will be sold and supported by Motorola as well as by Echelon. (To get a copy of Motorola's literature package, call your local Motorola sales office and ask for LONPAK/D.)

Toshiba makes the same device under license from Echelon, and calls it the TMPN3150F. Motorola prices the chip at $11.78 in quantities of 1,000; Toshiba quotes $12 in quantities of 50,000. Pricing is expected to drop to under $5 over the next three years, as the chip is moved to a denser process and then redesigned as a full-custom device to minimize the die size.

Motorola has also announced plans to invest $20 million in Echelon Corp. over the next 12 months, representing a 19% ownership position. This brings the company's total capitalization to $50 million. Motorola president Gary Tooker was elected to a seat on Echelon's board.

Zilog Targets Telephone Answering Machines

The latest trio of Z8-based microcontrollers from Zilog includes an on-chip DSP for telephone answering machines and similar applications. They're similar to the Z86C94 (see µPR 9/4/91, p. 1), but they use a different Z8 core that lacks the 16-bit integer multiply/divide unit. They also use a different version of the Clarkspur DSP design, in which the full 16-bit DSP instruction set is available. (Clarkspur is a small, San Jose-based design house that has licensed its DSP core to several semiconductor vendors.)

The Z89C65, Z89C66, and Z89C67 each provide 24K bytes of Z8 ROM, 256 bytes of Z8 RAM, 4K 16-bit words of DSP instruction ROM, and 512 16-bit words of DSP data RAM. Zilog expects most customers to use Zilog-supplied DSP application code, but it is making available a development system that combines a Z8 ICE system with a Clarkspur ICE chip for executing user-developed DSP code.

The Z89C65 is the cheapest version ($6.75/100K), intended for low-end, tape-based machines. The Z89C66 is slightly more expensive ($8/100K) and includes an external ROM interface and two parallel I/O lines. The high-end Z89C67 ($8.75/100K) adds an external audio-RAM (ARAM) interface and two DSP-controlled serial CODEC interfaces. The latter chip is intended for two-line machines with digital voice storage.

Sampling of the Z89C65 and Z89C66 is planned for January, with volume production in March. Samples of the Z89C67 are planned for March, with production in May. Zilog's new chips join National's 32AM160 and a chip set from the DSP Group in addressing the emerging market for digital answering machines.

Hitachi Reintroduces H8/500 Family

Hitachi's H8/532 microcontroller, originally introduced in November, 1988, is back on the U.S. market after a litigation-induced hiatus. Shortly after Hitachi first announced the H8/532, Motorola sued them for patent infringement. (Motorola and Hitachi had worked together in the past on 680x devices, but the two companies are now about as friendly as Intel and AMD.) Hitachi countersued, claiming that Motorola's 68030 infringed an Hitachi patent, and both the 68030 and the H8/532 were briefly banned from sale by the court. Faced with the collapse of key product lines, the two companies finally managed to talk to each other and come to an agreement, whose terms were not made public, in mid-1990.

Part of the secret agreement was apparently a provision that Hitachi would withdraw its H8/532 from U.S. marketing until January, 1992. Now that date has arrived, and the device is back on the market.

The H8/532 is part of the H8/500 family, which now includes five devices. All five are in production now in 6-, 8-, and 10-MHz versions. (Note that it is distinct from the H8/300 series, which is aimed at lower-cost applications and is not binary-compatible.) The H8/510 ROM-less device provides a dedicated expansion bus, so unlike the other family members, adding off-chip memory doesn't use up any I/O ports. This chip also includes a DRAM controller, since it is designed for large-memory applications. The H8/520 is the low-end device, while the H8/536 fills out the high end with an astounding 62K bytes of on-chip program memory. Each device is available with a mask-programmed ROM or a one-time programmable EPROM (ZTAT, or zero turn-around-time, as Hitachi calls it). Prices for masked-ROM versions range from $11.45 to $19.40 in quantities of 10,000, while the ZTAT versions sell for $22.25 to $34.10 in quantities of 1,000.

The H8/500 series is designed as a more modern competitor to the 6801, 6805, NEC's 78000 series, and other mid-range to high-end 8-bit microcontrollers, and it is claimed to offer better high-level-language support. It is, in fact, a 16-bit architecture with an 8-bit external bus, but Hitachi is positioning it as an alternative to 8-bit devices. It is considerably faster than its competitors, offering a 200-ns basic instruction time at 10 MHz and a 1.4 µs multiply. The devices also offer large program memories and cost-effective ZTAT versions, making them practical in single-chip configurations even for low- to moderate-volume applications. The biggest drawback is that the H8/500 family implements a new, sole-sourced architecture, so Hitachi must fight the inertia of existing designs and the hesitance of designers to use a sole-sourced part. ♦