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AT&T Sampling Low-Power "Hobbit" Processor

Second-Generation CRISP Design Targeted at Pen-Based Systems

By Michael Slater

AT&T has begun sampling a new, low-power microprocessor, called "Hobbit," that is derived from its earlier "CRISP" design and is likely to be the primary RISC platform for GO Corp.'s PenPoint operating system. AT&T has been briefing prospective customers under non-disclosure but would not officially confirm the existence of the chip or comment on any plans to market it. Reliable sources have confirmed, however, that the chip has been sampling since early 1991 and will target portable, pen-based products. Until now, the only RISC processor focusing on low power consumption has been the ARM, which is being used by Apple for its future pen-based systems.

Apple has, in fact, been a driving force behind both ARM and Hobbit, and corporate politics have played a major part in the development of both processors. The CRISP (C-machine Reduced Instruction Set Processor) architecture was developed by AT&T, starting in the early '80s, as an execution engine optimized for C-language programs. AT&T had previously developed its own 8-bit CISC microprocessor, the MAC-8. A 32-bit successor to that device, called the WE32000, was used in AT&T's computer systems in the early '80s; a second-generation version, the WE32100, was produced in 1986 (about the same time as the first CRISP chip) and was incorporated into AT&T's 3B2 computer systems. AT&T decided to stick with the WE32000 family (not to be confused with National's NSC32000 family), rather than building systems based on CRISP.

After one more processor generation (the WE32200), AT&T's computer systems group decided to throw in the towel on building its own microprocessors. Dave Ditzel, one of the lead architects of CRISP, joined Sun after AT&T's decision to abandon microprocessor development and has led Sun's advanced development efforts. AT&T initially planned to use the SPARC architecture, but later changed course again and is now using the MIPS R3000 to upgrade its existing systems.

While AT&T's computer operation gave up on CRISP, AT&T Microelectronics quietly pitched the chip to a number of prospective major customers. In early 1988, Apple paid AT&T an undisclosed figure (rumored to be $6 million) to develop a low-power, second-generation version of CRISP (Apple CRISP?) for use in Apple's pen-based system, code-named Newton. This was a pet project of Jean-Louis Gassee, and when Gassee left, Apple's VP of the Advanced Products Group, Larry Tesler, decided to switch to ARM. In the fall of 1990, Apple joined with VLSI Technology and Acorn Computer to spin the processor design operation out of Acorn into Advanced RISC Machines Ltd., which subsequently developed the ARM600 to Apple's specifications. This left AT&T with completed silicon for an enhanced version of CRISP, but without a customer for it.

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Meanwhile, GO Corp. was developing its pen-based operating system, PenPoint, and was looking for a low-power RISC processor as an alternative to Intel's x86. While GO has stated its intent to support other processor architectures, it has not publicly committed to any RISC architecture.

GO originally planned to develop both hardware and software, but the company later decided to focus on its operating system and act as a software supplier to numerous hardware vendors. GO built prototype pen-based systems using 286 and 386 processors to serve as development and demonstration vehicles, but the decision to abandon the hardware business left GO's hardware design team without a clear future.

In mid-1991, EO Computer was founded with backing from the venture-capital firm Kleiner Perkins (which also funded GO) and AT&T. EO's staff reportedly includes GO's former hardware design team. The company is currently led by Bernie Lacroute, a general partner at Kleiner Perkins, who was formerly Executive VP of Sun Microsystems and was involved in starting HaL Computer Systems. VP of marketing is Alain Rossman, who held the same position at C-Cube Microsystems, was a cofounder of Radius, and managed third-party developer relationships at Apple. EO acquired Active Book, a small U.K.-based firm led by Herman Hauser, one of the founders of Acorn Computers, who serves as EO's chief technical officer and is running a design operation that will remain in the U.K.

Address Type	Mnemonic	Function
2 and 2-1/2 Address	add	addition
	sub	subtraction
	mul	multiplication
	quo	division
	and	bit-wise AND
	or	bit-wise OR
	xor	bit-wise XOR
	shr	arithmetic shift right
	ushl	unsigned shift left
	ushr	unsigned shift right
2 Address	umul	unsigned multiply
	uquo	unsigned divide
	urem	unsigned remainder
	cmp.=	equality comparison
	cmp.s<	signed less-than comparison
	cmp.u<	unsigned less-than comparison
	move	move
	mova	move effective address
	addi	interlocked bit-wise add
	andi	interlocked bit-wise AND
	ori	interlocked bit-wise OR
1 Address	jmp	unconditional jump
	ifTjmp	unconditional jump if True
	ifFjmp	unconditional jump if False
	ifCjmp	unconditional jump if Carry
	ifOjmp	unconditional jump if Overflow
	call	procedure call
	kcall	kernel call
	enter	allocate new stack space
	return	de-allocate space and return
	catch	restore stack cache
0 Address	nop	no operation
	cpu	internal register access
	kret	kernel return

Table 1. CRISP instruction set summary.

Active Book had developed prototype systems using the ARM processor, and this work has now been scrapped in favor of Hobbit. It is ironic that Apple funded the development of Hobbit and then switched to ARM, while Herman Hauser created ARM and has now switched to Hobbit. With AT&T as the primary backer, it isn't hard to see why EO made its processor choice; the motivations for Apple's switch are less clear.

EO Computer declined to discuss its product plans, but reports indicate that the target product is a communications-oriented, pen-based computer. EO's product is apparently in the same "personal intelligent communicator" category used to describe products being developed by General Magic, a startup staffed with Apple alumni and backed by Apple, Sony, and Motorola. This market area is a natural fit for AT&T, which has been far more successful as a communications company than as a computer company. Such products could have a far wider market than general-purpose notebook computers, since they would be smaller, less expensive, and easier to use. Many more people need to communicate than need to compute.

The CRISP Architecture

Although it never emerged as a commercial product, the original AT&T CRISP design is well documented in a variety of conference papers (see box). First silicon was fabricated in the spring of 1986, using 1.75-micron CMOS and incorporating 172,163 transistors. It ran at a clock rate of 16 MHz and achieved a performance of 13,560 Dhrystones. A revised design was fabricated in early 1987 and turned in a performance of 16,950 Dhrystones at 20 MHz.

The CRISP instruction-set architecture is quite unusual. Table 1 shows the instruction set summary. CRISP is a memory-to-memory architecture, with no programmer-visible registers. Most computation instructions are available in two different forms: a two-address form, in which one address specifies one operand and the other is used both for the other operand and for the result; and a "two-and-a-half" address form, in which the two operands come from selected memory locations and the result is written to the top of the stack.

Instead of conventional registers, CRISP imple-

ments a stack cache. This is a group of on-chip registers that transparently stores the active section of the stack; it is 128 bytes in CRISP, and 256 bytes in Hobbit. It is similar in concept to SPARC's register windows, but it is more flexible because it has no concept of a fixed-size window. AMD's 29000 implements a similar stack cache in its register file, although its operation was simplified to reduce the implementation complexity.

Data types supported are 32-bit words, 16-bit halfwords, and 8-bit bytes; memory is byte-addressable, but misaligned halfwords and words are not supported. Addressing modes are immediate, absolute, stack offset, and stack offset indirect.

Instead of a traditional condition-code register, CRISP uses a single "true/false" bit that is set by explicit compare instructions. Arithmetic and logical instructions also set "sticky" carry and overflow bits.

CRISP uses variable-length instruction encoding. To ease decoding, the first two bits of all instructions encode the length, which can be two, six, or ten bytes. The ten-byte (80-bit) format allows two 32-bit constants (typically addresses) to be encoded in the instruction. The six-byte format supports instructions with two 16-bit constants or one 32-bit constant.

The most compressed, two-byte format was designed by selecting the 32 most-frequently-occurring opcode and addressing-mode combinations, determined by compiling the UNIX source code and analyzing instruction frequency. In the six- and ten-byte formats, which allow all possible opcodes and addressing modes, 14 bits are required to encode this information. In the two-byte format, only the 32 most-common combinations are supported, enabling this information to be encoded in a single 5-bit field. The two-byte encoding supports either two 5-bit operands or a single 10-bit operand. AT&T's papers claimed that 80% of instructions typically fit in the two-byte encoding. The short average instruction size, combined with elimination of register load and store instructions, is claimed to create a code density twice that of traditional RISCs.

Figure 1 shows a block diagram of the original CRISP chip. The instruction prefetch buffer is a traditional instruction cache. In the original implementation, this buffer is 512 bytes; in the Hobbit design, it is increased to 3K bytes and is three-way set-associative. The prefetch decode unit attempts to decode instructions ahead of the execution unit's need for them, and the decoded form is stored in the decoded instruction cache, which has 32 entries of 192 bits each in both implementations.

CRISP implements *branch folding* to reduce the cost of branches. The decoded instruction cache includes two next-address fields, allowing every instruction to include a branch. When an instruction followed by a branch is detected by the instruction decoder, it stores the branch target address in the next-address field of the preceding instruction, eliminating the branch instruction. An alternate next-address field allows conditional branches to be folded as well, and a static branch prediction bit controls which of the addresses is used.

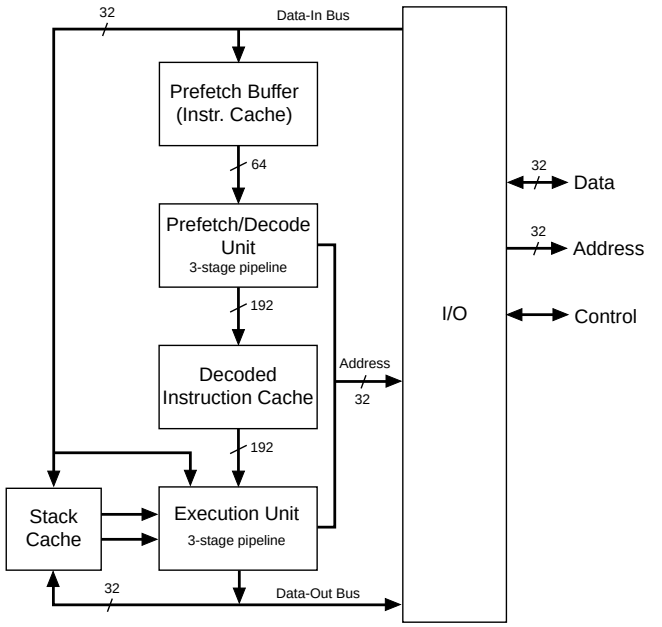

Figure 1. Block diagram of the CRISP microprocessor.

In addition to the increased cache sizes noted above, the Hobbit chip adds two 32-entry TLBs for memory management: one for instructions and one for data. The instruction set was extended with tagged arithmetic instructions and floating-point instructions, although the floating-point instructions are simply trapped in the current implementation. While CRISP was a big-endian machine (i.e., it stores the most-significant byte first), Hobbit supports both byte orderings as selected by a configuration register bit. The Hobbit chip is packaged in a 132-pin PQFP, and provides non-multiplexed, 32-bit address and data buses.

The chip is fully static, and is designed to run at 20 MHz with a 3.3-V power supply; power consumption is about 400 mW. Higher clock-rate versions are also planned. It is currently implemented in an 0.9-micron CMOS process, far denser than the 1.75-micron process used for the original device, and a shrink to an 0.7-micron process is planned. Price of the chip is expected to be about $50 in volume.

Conclusions

Inevitably, the question "Is this a RISC?" will arise, and the answer, of course, depends on your definition of RISC. Like classical RISCs, CRISP has a small instruction set with few addressing modes, and its features were designed to support compiler-generated code and

For More Information

Aspects of AT&T's original CRISP microprocessor design are described in numerous conference papers and journal articles. Listed below are several of the papers.

"A Pipelined 32b Microprocessor with 32Kb of Cache Memory," Alan D. Berenbaum et. al., *Proceeding of the International Solid State Circuits Conference*, February 1987.

"Introduction to the CRISP Instruction Set Architecture," A. D. Berenbaum, D. R. Ditzel, and H. R. McLellan, *Compcon 87 Proceedings.*

"Architectural Innovations in the CRISP Microprocessor," A. D. Berenbaum, D. R. Ditzel, and H. R. McLellan, *Compcon 87 Proceedings.*

"The Hardware Architecture of the CRISP Microprocessor," A. D. Berenbaum, D. R. Ditzel, and H. R. McLellan, *Proceedings of the 14th Annual Symposium on Computer Architecture*, 1987.

"Branch Folding in the CRISP Microprocessor: Reducing Branch Delay to Zero," D. R. Ditzel and H. R. McLellan, *Proceedings of the 14th Annual Symposium on Computer Architecture*, 1987.

AT&T has not yet publicly acknowledged the existence of the Hobbit processor, but if you're a prospective customer—and are willing to sign an NDA—you may find them more forthcoming. Contact AT&T Microelectronics in San Jose at 408/452-3966.

EO Computer is located at 800A East Middlefield Rd., Mountain View, CA 94043-4031; 415/903-8100; fax 415/903-8190.

pipelined processor implementations. Most instructions execute in a single clock cycle. Given its memory-to-memory architecture and variable-length instructions, however, calling it a RISC architecture seems like a stretch. On the other hand, it is not similar to conventional CISC processors, and the predecoded instruction cache presents the execution unit with RISC-like, fixed-length instructions.

Pen-based consumer electronics products promise to be one of the most exciting microprocessor application areas for the 1990s. The pen-based interface enables the system to be scaled down to sizes at which keyboards are awkward and impractical, and with the appropriate software, it can significantly improve ease-of-use and thereby widen the potential market. When combined with emerging wireless communication capabilities, the opportunity is enormous.

From a microprocessor perspective, this new application area represents a rare chance for new architectures to break into the market. Because the application and operating system software are new, the usual constraints imposed by the desire for compatibility with an existing software base are eliminated. The current crop of pen-based systems, in an 8.5" × 11" form factor, are predominantly 386-based because of the desire to run Microsoft's Windows for Pen Computing, as well as existing non-pen-based software if a keyboard is added, as well as PenPoint. While these machines will find market niches, the highest volume potential is in wallet-sized products that will need new application software.

The focus of the mainstream RISC players on the workstation market has left an opportunity for new designs aimed at portable applications. These applications don't really need a new architecture, but they do need inexpensive, highly integrated, low-power implementations. The fact that such implementations have been done for ARM and CRISP, but not for SPARC or MIPS, for example, has given these architectures an opening. Intel and Motorola might have been able to address this market with their CISC architectures, but they simply have not provided competitive performance, cost, or power consumption.

Hobbit's primary architectural advantage over other RISCs is its higher code density, which will be important for early portable products because it will decrease the memory requirements. As memory density continues to skyrocket, this will become less of an issue, but by that time a software base will have emerged and the dominant architectures for this market will be established. The stack cache also gives Hobbit a potential edge in system power consumption, since it reduces the number of memory accesses.

Just as the IBM PC made the 8086 architecture a success, the success of ARM and Hobbit will be determined by the products that incorporate them. The architectural differences between the two designs, while significant from a computer architect's viewpoint, are likely to be very minor when compared to the differences in the hardware and software products that incorporate these chips. Until details of the products from Apple, General Magic, EO Computer, and others become available, it is impossible to gauge the relative chances for success of the two processor architectures.

ARM has the advantage of an existing market presence and multiple sources (GEC Plessey recently signed up to supply the ARM processors), as well as the backing of Apple and, reportedly, Sony. ARM has suffered from a lack of software and development tools, as well as lackluster marketing, and it is not clear how much this situation will improve. AT&T's track record in marketing microprocessors is not very good either, however, and it remains to be seen what type of support they will provide and how aggressively the chips will be marketed. For the pen computing market, the strength of the partners each microprocessor vendor has lined up could be the most important factor. ♦