Wave of High-End Processors Due

Most in 40–80 SPECmarks Range, 16–36K On-Chip Cache

By Michael Slater

After two years of being stuck in the 20–30 SPECmark range, high-end microprocessors will move up to the 40–80 SPECmark performance level in 1992. As a result, a new wave of workstations and high-end PCs will emerge with two to four times the performance of existing models.

MIPS is in the lead in delivering this generation of silicon, with the R4000 now on the verge of volume production. TI's SuperSPARC and Motorola's 88110 are likely to be next out the gate, with Intel's P5 promised to follow by the end of the year. Samples of the first PowerPC chip from Motorola are also promised for late this year, but this chip won't achieve the same performance levels as its competitors. HP and DEC will also ship next-generation RISC processors this year, although it is not clear whether either chip will be available on the merchant market.

R4000 Moving Into Production

MIPS has been shipping R4000 samples since last September, and the revision 2.0 silicon is now being evaluated. Expectations are that the 2.0 design will go into production in the next month or two, and that it will be suitable for both the R4000PC (no secondary cache) and R4000SC (secondary cache) configurations. It is also being used for multiprocessor prototypes, and the R4000MC (multiprocessor) version is expected to be in production by mid-year.

MIPS has not yet released any measured performance numbers for the R4000. SGI is claiming a 70-SPECmark rating for its R4000-based system, well above the 62 SPECmark figure from simulations, but SGI has not provided the individual SPEC benchmark figures to back up this claim. Most of the increase is probably due to continuing compiler tweaks, rather than to any improvement in the chip itself, although the 2.0 silicon does include some minor performance enhancements.

Later this year, the MIPS semiconductor partners plan to push the existing R4000 design to 75 MHz (100 MHz internal). In addition, a revised design with twice the on-chip cache is expected by late this year or early in '93. These new versions will be critical to keeping the R4000 competitive, since the current design will be outpaced by both SuperSPARC and Motorola's 88110.

Low-end MIPS-based systems will begin shifting from R3000-based designs to the integrated designs, such as IDT's R3081 and Performance Semiconductor's PIPER, that combine the processor, FPU, 10K to 20K bytes of cache, and a read/write buffer in a single chip. These devices should enable system makers to reach lower prices than ever before for RISC-based systems.

Waiting for SuperSPARC

Last fall, the long-rumored Texas Instruments/Sun "Viking" SPARC processor was publicly acknowledged as SuperSPARC, and a general description of the chip was given at the *Microprocessor Forum* (see µPR 12/4/91 p. 22). With 3.1 million transistors and 36K bytes of on-chip cache, SuperSPARC is the most aggressive RISC microprocessor implementation yet described. A formal announcement of the chip is expected late this spring, in concert with Sun's announcement of systems using it.

SuperSPARC is likely to be used in Sun's future high-end workstations, and it should enable Sun to compete with IBM and HP in the performance-oriented parts of the market. For the past year, Sun has been at a significant disadvantage in this area.

Cypress/ROSS Technology has yet to make any announcements regarding its next-generation SPARC processor, called Pinnacle. Cypress/ROSS has been remarkably slow in introducing new products; the original 7C601, designed in 1987 in collaboration with Sun, remains its only processor (except for the 7C611, a packaging variation for embedded applications), and the supporting cache/memory-management chips were shipped far behind schedule. The only design win at Sun for the ROSS chip set is in the "Galaxy" multiprocessor server. This system was originally supposed to use SuperSPARC, but delays in that project gave ROSS a window of opportunity.

Pinnacle was originally expected to ship before SuperSPARC, but it now appears that it will be at least six months later—despite SuperSPARC's own schedule slips. The first official peek at Pinnacle will come at Compcon later this month, where ROSS architect Raju Vegesna will give an overview of the Pinnacle design. Performance, pricing, and availability will not be discussed, however, and production doesn't seem likely until late this year at best.

While SuperSPARC and Pinnacle push SPARC up in performance, these processors won't be inexpensive enough for a $5000-class workstation in the next year or two. After completing the original Fujitsu gate-array SPARC integer unit and the Cypress full-custom imple-

	Architecture	**PA-RISC**	PA-RISC	**RS/6000**	RS/6000	R4000PC	88110	SPARC	486
	Clock Rate (MHz)	**35**	50	**33**	33	50/100	50	33	50
	External Cache	**32K + 64K**	32K + 64K	**none**	8K + 64K	none	none	64K	256K
	System	**HP 705**	HP 710	**IBM 220 (RSC)**	IBM 340 (Multichip)	Simulated	Simulated	Sun ELC	Compaq Deskpro
Integer	gcc	**19.6**	29.0	**14.6**	26.0	28.0	46.5	20.0	31.0
	espresso	**28.3**	39.8	**19.7**	27.3	39.0	48.1	21.7	24.6
	li	**25.4**	36.7	**14.7**	28.4	45.3	57.0	23.1	33.9
	eqntott	**26.0**	37.2	**22.0**	34.2	50.1	52.9	22.3	22.3
Floating Point	spice2g6	**22.9**	33.2	**14.6**	34.0	28.0	34.7	16.5	17.5
	doduc	**29.7**	42.5	**18.1**	38.8	36.2	41.4	18.2	11.1
	nasa7	**35.6**	51.7	**32.3**	103.0	43.2	67.9	29.1	18.5
	matrix300	**190.9**	277.6	**191.5**	524.1	177.3	357.8	82.6	17.5
	fpppp	**32.8**	45.3	**25.7**	69.4	36.2	64.4	23.8	15.5
	tomcatv	**43.9**	64.1	**34.7**	98.7	37.3	72.2	24.9	12.6
Geometric Means	SPECmark89	**34.6**	49.7	**25.9**	56.6	43.8	63.7	25.0	19.3
	SPECint89	**24.6**	35.4	**17.5**	28.8	39.7	51.0	21.7	27.6
	SPECfp89	**43.4**	62.4	**33.7**	88.7	46.8	73.9	27.4	15.2

Table 1. SPEC89 results for IBM's and HP's new low-end systems. Also included for comparison are IBM's 33-MHz system using the multichip processor, the low-end R4000 configuration, the 88110, Sun's current low-end SPARC system, and a top-of-the-line 486 system. (Note that SPEC89 is the new designation for the original SPEC suite; IBM and HP also provided SPEC92 numbers, but we've used the older suite because more comparative numbers are available.)

mentation, Sun focused its efforts on high-performance, superscalar implementations without first building a more modest, but fully integrated design. To compare to the Intel line, Sun decided to go from a 386-like processor to a 586-like design, skipping over the 486 level of integration. Both Fujitsu and Weitek produce a combined integer/floating-point chip, but this device still requires an external MMU and cache controller.

To provide Sun with a cost-effective processor for its future low-end workstations, Fujitsu is rumored to be developing a highly integrated processor, adding an MMU, cache, and other functions to the existing IU/FPU chip. LSI Logic would also be a natural candidate to develop such a chip. These integrated SPARC processors could incorporate other system functions, such as a DRAM controller, peripheral bus interface, or SBus interface. Texas Instruments is also rumored to be developing a highly integrated SPARC chip, code-named Genie, that includes a frame buffer controller.

Lightning Dies, but Thunder Coming

The third anticipated high-end SPARC chip, LSI Logic's Lightning, is now officially dead—LSI VP Brian Halla confirmed that LSI has abandoned its plans to produce this processor. Halla said that the SPARC-compatible system market was not developing as they had expected, and that there was relatively little interest in processors that Sun wasn't planning to use. With Sun's commitment to SuperSPARC, this left insufficient market to justify completing the project. Other sources indicated that the complexity of the chips may have strained LSI's fabrication capability. The collapse of the Lightning project is reminiscent of Fujitsu's ill-fated SPARC-H, a high-end SPARC design that Fujitsu canceled when Sun decided not to use it because of schedule slips and questions about its performance. SPARC seems to have suffered from more than its share of canceled and delayed processor projects, due in large part to the existence of more processor development projects than the market can support.

Halla said that LSI remained committed to the out-of-order, speculative execution technology that was the heart of the Lightning design, but that it would be applied to other instruction set architectures. The technology eventually may appear as part of LSI's core processor program for ASICs, which will be announced later this month.

Metaflow Technology, which created the Lightning design for LSI Logic with funding from Hyundai, is now working on a faster, next-generation implementation called Thunder. Unlike Lightning, this will be a full custom design, and it will be fabricated by an unnamed foundry—not LSI Logic. The project is backed by Hyundai, which plans to use it in a line of SPARC systems.

Bipolar Integrated Technology's ECL SPARC processor did make it into production, but it has had very little success. With SuperSPARC on the verge of shipping, the ECL chips look even less attractive; not only is the level of integration low, but power consumption is very high. The only announced customer is FPS Computing, which has been acquired by Cray Research and renamed Cray Research Superservers. In a major boost to Sun's "laptop to supercomputer" pitch, Cray has announced plans for a new SPARC server to be delivered in late 1993 and priced in the $1–3 million range. Cray officials would not discuss the hardware technology to

be used in these systems, but it seems unlikely that they will continue to use BIT's ECL processor.

The specification for the 64-bit version of SPARC may emerge in 1992, but chips aren't likely to be available on the merchant market until 1993 at the earliest. HaL Computer Systems is developing its own proprietary implementation of that architecture, and it is expected to ship systems by year-end.

RS/6000 and PowerPC

IBM continues to broaden its RS/6000 line, having announced last month both a low-end system using the RIOS single-chip (RSC) processor and a high-end system using the original multichip set running at 50 MHz. (RIOS is IBM's internal name for the RS/6000 processor.) The performance of the single-chip implementation is unexciting, however, due in part to the relatively tiny on-chip 8K instruction and data cache.

As Table 1 shows, the 33-MHz RSC turns out a SPEC integer performance of only 17.5—slower than a 486 at the same clock rate, and substantially slower than the 27.6 SPEC integer performance of a 50-MHz 486. The SPEC floating-point performance of 33.7 is much better than the 50-MHz 486's rating of 15.2, but on some of the individual floating-point benchmarks the performance of the two is much closer. (One unfair aspect of this comparison is that the RSC system uses no external cache, while the 486 system has a 256K-byte external cache.)

The RSC also fares poorly when compared to the R4000 and 88110, but these chips are not yet in production and IBM will have faster versions of the RSC soon after those chips begin shipping. IBM's initial RSC-based system was designed with a low-cost focus, and there are several clear opportunities—such as increasing the clock rate and adding an external cache—to boost the performance.

As the comparison to the multichip implementation at the same clock rate shows, the low-end system has dramatically lower performance per clock cycle. Many factors contribute to this, including the smaller cache, slower floating-point unit, more restricted superscalar capabilities, and narrower path to main memory.

Figure 1 shows a die photo of the RSC. IBM uses a compiled, semicustom design approach that enables them to create designs quickly but does not produce very compact layouts. The chip is fabricated in IBM's CMOS-2S process, which uses 0.9-micron lithography and has an effective gate length of 0.5 microns. At 344K square mils, the RSC is 35% larger than Intel's original 1-micron 486 design, which has the same size cache and approximately the same transistor count; it is over 2.5 times the size of Intel's 0.8-micron version of the 486. With Intel's higher volumes, they can justify a much larger investment in packing the design tightly. As part of the PowerPC program, IBM hopes to achieve the volume levels needed to justify this type of design, and Motorola will provide the required expertise.

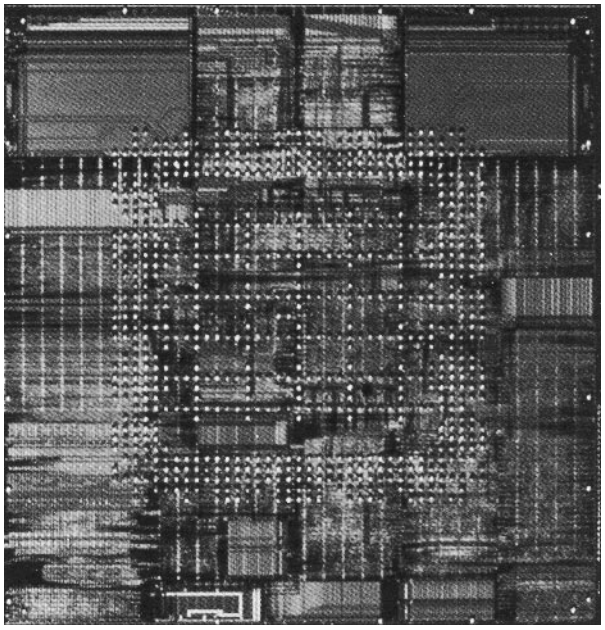

Figure 1. Die photo of IBM's 1.2-million-transistor RSC, which measures 15.2 x 14.6 mm (600 x 575 mils).

The RSC has 201 signal lines, including a 64-bit memory bus and a 32-bit I/O bus. Full ECC is provided for the memory bus, and there is a four-word write buffer. At 33 MHz, it consumes about 4 W. Like IBM's multichip design, the chip core runs at 3.6 V, but all I/O is TTL-compatible.

The RSC maintains the independent fixed-point, floating-point, and branch units of the multichip implementation (see µPR 8/21/91, p. 10), and it implements the full POWER instruction set. It provides hardware support for misaligned data accesses, string operations, and load/store multiple instructions.

Several simplifications were made to the microarchitecture of the multichip design to reduce the transistor count and enable a single-chip implementation. For example, both the multichip design and the RSC fetch four words at a time from the cache to the fetch/decode unit. While the multichip implementation examines a five-instruction window and can dispatch up to four instructions per cycle, however, the RSC uses a three-instruction window and can dispatch only two instructions per cycle.

Another simplification is that the instruction fetcher operates autonomously only within a 4K page, and branches can be processed concurrently with fixed-point instructions only if they are within a page. The multichip design has a fully autonomous branch unit and prefetcher, but the RSC requires use of the fixed-point unit for address calculations when a page boundary is crossed.

While the multichip design has a double-precision floating-point data path, making double-precision just as fast as single-precision, the RSC does not. A double-

precision multiply-add can be started every two cycles, instead of every cycle, and has a five-cycle latency.

The 8K unified (instruction and data) cache is two-way set associative, and uses a write-through memory update policy. Cache lines are 64 bytes each and are divided into four sectors. Hardware cache coherency is provided for DMA transfers on the I/O bus, a feature that is not present in the multichip design.

The I/O sequencer is a microcode engine dedicated to handling the I/O bus. This sequencer implements a DMA controller, 16-input interrupt controller, TLB table walking, a real-time clock, power-on reset, and self-test. It is designed to simplify the interface to the Micro Channel and minimize the external logic required for system control functions.

The first PowerPC chip will be derived from the RSC design. (See µPR 12/26/91 p. 1 for IBM's PowerPC roadmap, and p. 9 of that issue for details on the PowerPC architecture.) This chip, to be called the 601, will eliminate the separate I/O bus interface and replace the memory interface with a bus similar to that on Motorola's 88110. The I/O sequencer will be eliminated, and the cache size will be increased. The chip will also be modified to incorporate the PowerPC architectural changes, which will also help increase the clock rate by shortening some critical timing paths. It will be implemented in IBM's next-generation process technology, and IBM expects it to run at over 50 MHz. These changes will boost the RSC's performance substantially, but it is not likely to match the performance of the 88110 or the R4000, at least when the R4000 moves up to 75 MHz.

IBM's recent licensing of Power and PowerPC to Groupe Bull in France provides the first tangible results of IBM's campaign to find additional licensees for its RISC designs. As with the Apple design win, business considerations overwhelmed any concerns about modest performance of the initial chips. Microprocessor choices are often political, but in the case of Bull it was truly so—the top ministers in the French government (which owns most of Bull) were deeply involved in the decision.

PA-RISC to Maintain FP Lead

Hewlett-Packard's PA-RISC architecture rose to prominence in the workstation world last year by leapfrogging its competitors' performance levels, and HP expects to maintain this lead in 1992. HP's recently announced low-end systems don't include any new processor technology; they are based on the same "Snakes" chip set used in the original Series 700 products, but with smaller caches and lower clock rates. While the original systems have 128K for instructions and 256K for data, the new models 705 and 710 have a 32K I-cache and a 64K D-cache. The 710 runs at 50 MHz, while the 705 is scaled back to 35 MHz. As Table 1 shows, even HP's Model 705 is significantly faster than IBM's low-end system, despite the fact that IBM's design is superscalar and HP's is not—a testament to the value of larger caches.

At Compcon later this month (see p. 24), HP will describe its first superscalar PA-RISC implementation. Continuing its emphasis on high clock rates, the chip is designed to operate at 100 MHz—in production systems, not just for conference presentations. This chip was designed entirely by HP; it does not use TI's floating-point processor that is part of the Snakes chip set, and Hitachi was not involved.

The new device combines the integer and floating-point units on a single chip, but it does not include any on-chip cache. It is a two-issue superscalar machine, limited to one integer and one floating-point instruction per cycle. Loads and stores, however, are considered integer operations, even if the destination is the floating-point register file. As a result, a floating-point load or store can be issued at the same time as a floating-point computation instruction.

In addition to the dual-issue capability and higher clock rate, the new processor's FPU is capable of twice the peak issue rate of the Snakes design: it can start a multiply and add every cycle, while the Snakes design has a two-cycle issue rate. Considering the combination of the fast FPU, high clock rate, and dual-issue capability, and in light of the already impressive performance of the earlier, less-capable implementations, this chip promises to be a floating-point screamer. Integer performance will be boosted by the high clock rate, but integer-only code will not gain any benefit from the superscalar issue capabilities.

HP will make the new processor available to its strategic partners (Hitachi, Samsung, Oki, and Sequoia Systems), but there are no current plans to make it available on the open market. Hitachi is shipping one of HP's older PA-RISC chips, but this device is too slow for the workstation market and not highly integrated enough for the embedded market. Hitachi has talked about plans for a high-end PA-RISC chip, but no product details have been released.

Motorola's 88110

Motorola's 88110 promises to be one of the fastest single-chip processor implementations to ship in 1992, but its market impact will be limited by lack of leading companies that are committed to it. (See µPR 12/4/91, p. 1 for details on the 88110.) If Motorola's claims are borne out, the 88110 will be considerably faster than the R4000, and its on-chip graphics unit should make it an especially potent chip for workstations. Despite the appeal of the IBM alliance, it is a shame that Apple won't be building 88110 systems, since it probably would have

given them a lead of at least a year over the first PowerPC chips and would have provided considerably higher performance. The 88110 isn't yet production-ready, however; sources indicate there are still serious bugs in the MMU.

Data General claims to remain firmly committed to the 88000 family. DG has not made much of an impact on the workstation business, but they have been successful in selling large multiuser systems for commercial applications. This may be fine for DG, but the volumes are too low to be of much interest to Motorola.

Most companies currently building 88000 products are likely to develop 88110-based systems, since it will give them very competitive performance, at least for the next year or two. In the long run, however, it seems inevitable that most companies using the 88000 will be shopping for a new architecture. Given the continued turmoil in the computer business, it makes sense for them to continue with the 88110 while they wait for the market to sort itself out.

NeXT is believed to be continuing development of its 88110-based system, in spite of its announced plans to provide its software for 486-based systems. Being out of the mainstream seems to be a way of life for Steve Jobs, and if you don't care about being in the mainstream the 88110 may well be the best choice for a high-end processor in 1992. It seems less likely that this will continue to be a good choice later in the decade.

In any case, NeXT has clearly decided to support multiple architectures. It has defined a "fat binary" format that allows developers to encapsulate multiple object-code versions into a single binary file, which can then be loaded and executed on any architecture for which object code is included. For most programs, much of the binary file is data, which does not have to be replicated for each architecture. NeXT claims that applications have been simple to port to the 486, with even complex applications ported in less than a week. In the near future, NeXT hopes that its application developers will begin including the 486 object code as well as the 680x0 code, and 88110 code may be added as well.

DEC's Alpha

The wild-card for 1992 is DEC's "Alpha" RISC architecture. The first implementation of Alpha will be revealed at ISSCC later this month, and we'll have a detailed analysis shortly thereafter. Alpha is a 64-bit architecture following a fairly pure RISC design philosophy. The initial chip is claimed to run at 200 MHz, and DEC is making grand claims about the architecture's superiority over all previous RISC designs.

System using Alpha aren't expected to be announced until the second half of the year, and the first systems will be aimed at high price/performance points. DEC's near-term application for Alpha will be as a VAX upgrade, not as a MIPS replacement, but there is no technical reason why it cannot replace the MIPS line as well. It might be years before Alpha systems reach the price points of R4000-based systems, but DEC's long-term commitment is clearly with Alpha.

If DEC does not manage this transition very carefully, it risks alienating its current and potential MIPS customer base before it has an alternative to offer them. Trumpeting the Alpha technology well in advance of availability must surely be causing serious resentment among DEC's managers responsible for developing and promoting MIPS-based systems. DEC's recent announcement that the MIPS-based workstation design team was being moved from the Palo Alto research center back to corporate headquarters in Massachusetts was also ill-timed, since many observers assumed this meant a phasing out of MIPS-based design activity—a charge that DEC denies. DEC is likely to continue developing MIPS-based workstations for some time, but pulling the design group back to headquarters nevertheless raises questions about the group's autonomy.

Intel's 860 Fading

Over the course of 1991, it became clear that Intel recognized that the 860 didn't stand a chance of penetrating the workstation market, and the 860 program has been significantly scaled back. While Intel did ship the second-generation 860XP, only the caches are significantly different from the first-generation implementation, and it is not clear how much Intel will invest in a next-generation 860 processor core. In the meantime, other architectures are catching up to the 860's floating-point performance and integration level, leaving it without a compelling reason to exist. Intel's biggest motivation to continue the line may be to avoid stranding those customers that have adopted it.

The 860 was introduced too late to penetrate the workstation market, and developing optimized software for it proved very difficult. The 860 is a prime example of what can happen when an architecture is defined without sufficient input from compiler or operating-system experts. The 860 missed its greatest opportunity—being the first RISC port of Windows NT—because the Microsoft software engineers attempting to use the chip came to hate it with a passion.

The one area where the 860 has been a significant success is in 3-D graphics accelerators. In this application, the processor runs a fixed set of graphics library functions, which can be hand-tuned to extract the optimum performance from the processor. Intel will have to aggressively advance the 860 line to hold on to this market, however. Other processor vendors are targeting this area, and since the processor used is invisible to application software, the benefits of incumbency are not nearly as great as in the PC business. An even more

Architecture	1990		1991		Growth
	Units	% Share	Units	% Share	90–91 (%)
SPARC	138,380	36.3	204,200	44.0	47.6
680x0	119,228	31.3	100,600	21.7	–15.6
MIPS	39,485	10.4	55,515	12.0	40.6
IBM POWER	16,405	4.3	25,846	5.6	57.5
HP PA–RISC	0	0.0	20,000	4.3	n/a
Clipper	14,470	3.8	13,000	2.8	–10.2
88000	6,490	1.7	4,000	0.9	–38.4
80x86	1,955	0.5	2,000	0.4	2.3
Other	44,873	11.8	39,000	8.4	–13.1
Total	381,286	100	464,161	100	21.7

Table 2. Workstation/workstation server shipments by procesor type. Note that these figures exclude both PCs and multiuser systems. (Source: International Data Corp., January 1992.)

ominous threat is the increasing performance of the main CPUs in workstations, which reduces the need for accelerated display controllers except in very-high-end (i.e., low-volume) applications.

The other area in which the 860 has had some success is in high-end multiprocessor systems, but Intel appears to be scaling back its efforts in this area as well. The much-heralded PAX loop-level parallelism scheme (see µPR 11/89 p. 6) appears to have died, as the support chips required to implement it have never appeared. Given the low unit volumes of this market, it is not surprising that Intel would question the justification for further investment.

Intel's management must also question whether promoting or investing in the 860 is a sensible thing for them to do in light of the expected high floating-point performance of the P5. With the relatively poor FP performance of the 486, the positioning of the 860 made more sense, but the P5 will erase much of the gap.

One area in which the emphasis on the P5 seems to have already had an impact is in support for the 860 as a 3-D graphics accelerator for x86-based PCs. Intel recently canceled development of a software package to provide a standard environment for 3-D applications, angering some add-in board makers.

Penetrating the PC Market

As Table 2 shows, SPARC continues to dominate the workstation market. All but about 15,000 of the SPARC shipments are from Sun, so the success of SPARC is, so far, really just the success of Sun. The most successful of the Sun-compatible system makers measure their shipments in hundreds of units a month—nowhere close to the volume that would make a business for a semiconductor supplier, much less several competing suppliers.

Table 3 shows Andrew Allison's estimates of RISC microprocessor shipments, including embedded processors and processors used in multiuser systems as well as workstation chips. Chip shipments are higher than workstation shipments not only because they include other applications, but also because they include chips in the distribution and system manufacturing pipeline. The two leading embedded RISCs—Intel's 960 and AMD's 29000—experienced the most spectacular growth, and this is likely to continue in 1992. (The transputer doesn't compete in the same market and isn't really a RISC, and it clearly does not have the momentum of the 960 and 29000 families.)

RISC processor shipments remain a small fraction of 386/486 shipments. While several competing RISC architectures fight over a market of a few hundred thousand units per year, Intel (and the growing ranks of Intel-compatible processor suppliers) shipped over 15 million 386 chips and well over 2 million 486 chips. Motorola's 68040 shipments, at about 260,000 units, were just over a tenth of Intel's 486 shipments.

Makers of RISC processors have been lusting after the PC market for the past several years, but their hopes remain unfulfilled. The key issues remain the cost of the systems and the availability of software. While workstations have come down to the $5000 range, typical configurations remain over $10,000, and the volume desktop computer market is for $2000 systems. And while more personal productivity software has become available for workstations, and graphical shells are making UNIX easier to use, the simple fact remains that a Macintosh or a Windows machine is still a better choice for most business desktop computer applications.

Sun has sought to create the impression that SPARC-based systems would mimic the success of the PC because Sun would encourage cloning of its workstations and the creation of a high-volume market. It is too early to call the clone strategy a failure, but it certainly has not produced meaningful results so far. This is due, in part, to Sun's lack of real commitment to its stated strategy. In reality, Sun is only interested in encouraging compatible systems if those systems are limited to niches that Sun doesn't want to address. Available SPARC chip sets have been one step behind Sun's products, and availability of complete, current system software has also been a problem. These difficulties are being addressed through SunSoft and the emergence of more advanced chip sets, but real growth in the SPARC market is most likely to come from Sun's own growth.

MIPS has based its hopes on the ACE initiative, and, in particular, on the ARC standard for MIPS-based systems that will run several flavors of UNIX as well as Microsoft's forthcoming Windows NT. Late last year, Microsoft began shipping a single CD-ROM developers' kit for Windows NT that includes code for the R4000 as well as the 386/486, marking the first time Microsoft has shipped a RISC-based software product and one of the first times a single distribution disk has supported multiple architectures. This is a very positive develop-

ment for MIPS, but it is not clear that it will be enough to make ARC systems a major success in light of the other challenges ACE members face.

Many of the major ACE participants are struggling, have a questionable level of commitment to ARC systems, or both. Compaq and SGI recently split up, apparently unable to agree on the features that their jointly-developed system should include. Compaq says it remains committed to making ARC-based systems, but given their shaky financial picture, the level of investment they can justify is questionable.

Architecture	1990		1991		Growth
	Units	% Share	Units	% Share	90–91 (%)
29000	85,000	10.2	300,000	21.1	253
SPARC	185,000	22.2	280,000	19.7	51
transputer	240,000	28.7	260,000	18.3	8
i960	65,000	7.8	250,000	17.6	285
MIPS	90,000	10.8	120,000	8.5	33
88100	50,000	6.0	85,000	6.0	70
ARM	55,000	6.6	65,000	4.6	18
i860	65,000	7.8	60,000	4.2	–8
Total	835,000	100	1,420,000	100	70

Table 3. RISC microprocessor shipments. (Source: *RISC Management* newsletter, January 1992.)

For the other PC vendors that have joined the ACE initiative, it seems to be little more than an insurance policy. The two companies that have demonstrated ARC systems are Acer and Olivetti. The systems Acer has demonstrated are based on the MIPS reference design, but Acer does not plan to produce this system. Instead, Acer will make a system with interchangeable CPU modules, allowing the user to install either a 486 (or perhaps P5) CPU card or an R4000 CPU card. Acer sees ACE as a way of offering its customers a choice of processors, and the company has little stake in the success of the MIPS-based configuration.

Perhaps the biggest challenge facing MIPS is Intel's success in creating the perception that the P5 will be faster than the R4000. If the reality matches Intel's claims and the P5 ships this year as Intel has promised, MIPS-based machines will have a difficult time competing head-to-head with P5-based systems.

Despite considerable strife within the initiative, ACE will produce meaningful results—such as the emergence of a standard MIPS platform, binary compatibility among most MIPS system vendors, and the porting of Windows NT to the MIPS architecture. Its major impact will be in the traditional workstation market, however, and it is not clear that PC users will see enough of a price or performance advantage in MIPS-based systems to give them a reason to select a MIPS-based system to run Windows NT.

The PowerPC may have the best chance of all the RISCs to penetrate the PC market, due in large part to Apple's commitment to moving its entire Macintosh line to that architecture. This will be a slow transition, however, and the PowerPC is likely to be little other than a development platform for Apple and its application developers until the middle of the decade.

Like the other RISC system makers, HP has hopes of penetrating the PC market with its PA-RISC systems. There is no apparent path for it to do so, however; its focus has been on floating-point performance, and it has no clear path to acquiring a base of personal productivity applications. HP should continue to do well in the performance-oriented workstation market, however, and this may, in fact, be a far safer strategy than the frontal attack on the PC market MIPS is attempting. If HP can keep its PA-RISC line advancing through profits from the technical workstation market, it may be able to last long enough to eventually become a player in the broader market when architecture-independent software standards emerge.

Intel remains firmly in control of the high-volume desktop computer market, and the threat from AMD and other 386/486-compatible processor makers is far greater than the threat from RISC processors. As system software suppliers have become impatient with the growth of the RISC market and Intel's processor performance has increased, almost all are targeting the 386/486 architecture as an alternative platform. Sun will offer Solaris for Intel; NeXT is porting NeXTStep; USL and Novell have formed Univel to offer SVR4 for Intel; the Apple/IBM "Pink" software will be offered on Intel as well as PowerPC; and even ACE includes a dual MIPS/Intel standard. No matter what operating system succeeds, x86-based systems will benefit. From a system buyer's perspective, this will make a P5-based machine an exceptionally safe choice.

The biggest weakness of Intel-based PCs has been their outdated system architecture and low-performance displays, but this is changing. The populariy of Windows has freed system makers to pursue display approaches that aren't bound by compatibility with IBM standards, and resolutions are creeping up to workstation levels. Several vendors, including DEC, have discovered that there is a market for Intel-based PCs with workstation-like configurations. With the emergence of more advanced system architectures, the P5, and multiple operating systems, the PC may pose a bigger threat to workstations than the workstations pose to the PC. (For more on this topic, see *MIPS and Sunset*, µPR 6/26/91 p. 12.)

In time, standards for source-level compatibility between x86-based systems and RISC-based systems will make it easy for software developers to support multiple processor architectures, and Intel's lock on the market will diminish. For the next year or two, however, and possibly for much longer, RISC processor vendors are unlikely to penetrate much of the x86 market. ♦