Ross Previews Pinnacle SPARC Design

Multichip Set to be Offered Only as a Module

By Michael Slater

Ross Technology (a subsidiary of Cypress Semiconductor) gave the first public preview of its Pinnacle-1 SPARC processor at Compcon last month. While the design has been rumored for years, Ross and Cypress have refused to acknowledge any aspect of the program until now. The company still will not discuss pricing, silicon status, or availability plans. The only performance estimate given was two to three times the performance of the current 40-MHz 7C601.

Figure 1 shows a block diagram of the Pinnacle-1 chip set. The design is unusual among next-generation high-end processors in that only an instruction cache (which is 8K bytes, two-way set-associative) is included in the processor chip. The processor works with a cache controller, memory-management, and tags unit (CMTU) that provides the 64-entry address translation cache (ATC, commonly called a TLB) and a controller for the off-chip combined instruction/data cache. This cache serves as the first-level data cache and a second-level instruction cache. This device is derived from the existing 7C605 CMTU, with enhancements to support 64-bit data paths and a faster processor interface. The MMU also includes a four-entry page-table pointer (PTP) cache that speeds ATC miss handling.

Because there is no on-chip data cache, there is a one cycle load-use penalty (i.e., if the instruction following a load uses the data from that load, there is a one-cycle stall, assuming a hit in the data cache). This is the same as for the existing 7C601 processor, but it is one clock cycle slower than SuperSPARC, for which there is no load-use penalty.

The cache memory itself is implemented with two or four 16K × 32 cache RAMs that Cypress/Ross is designing for use with the Pinnacle-1 processor but also plans to market for other applications. These RAMs include a one-level write buffer that allows them to process a write followed by a read without any timing penalty. Only two cache sizes are supported: 128K, using two SRAMs for low-end configurations, and 256K, using four SRAMs. The cache is virtually indexed and physically tagged, uses a direct-mapped organization, and has a 32-byte line size. It can operate in either write-through or copy-back modes.

The CMTU supports multiprocessor systems in accordance with the level-2 MBus specification, using a MOESI coherency protocol (see µPR 6/20/91, p. 12). It supports direct data intervention, in which the snooping cache provides data directly if it detects a snooping hit on a dirty cache line, and reflective memory, which means that memory is updated by the same bus cycle that transfers the data from one cache to another. The cache tags are fast enough to be accessed from both buses during every cycle, so MBus snooping does not contend with the processor for access to the cache.

The intra-module bus (IMB) connects the processor, CMTU, and cache RAMs. It is not accessible by other system components; all other devices must connect to the MBus interface, which is provided by the CMTU. The IMB has a non-multiplexed 32-bit address bus and 64-bit data bus. Since the IMB is private to the chip set, Ross is able to use non-standard logic levels to enable high clock rates. The CMTU has a 32-byte read buffer and a 64-byte write buffer that couple the cache to the MBus interface, providing clock-speed isolation. Ross would not disclose what it expects the CPU clock rate to be, but 66 or 75 MHz seems likely. Ross expects its performance to be close to SuperSPARC; although it has more limited issue capabilities and a smaller on-chip cache, Ross expects it to run at a higher clock rate.

The processor is in a 208-pin package, while the CMTU has 312 pins. Both devices are implemented in Cypress' 0.65-micron, two-layer-metal CMOS process, which was developed for 1-Mbit SRAMs. The processor is about 550 × 550 mils and includes approximately 1 million transistors, and the CMTU is about 450 × 450 mils and has about 700,000 transistors. The complete module comprises 12 million transistors.

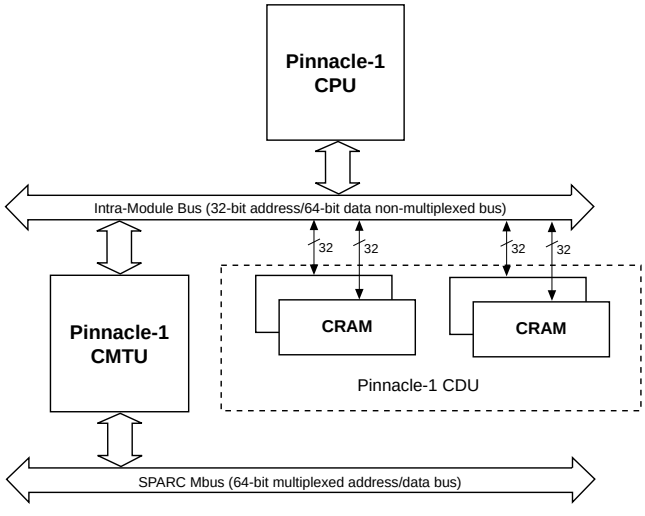

Figure 1. Block diagram of the Pinnacle-1 chip set.

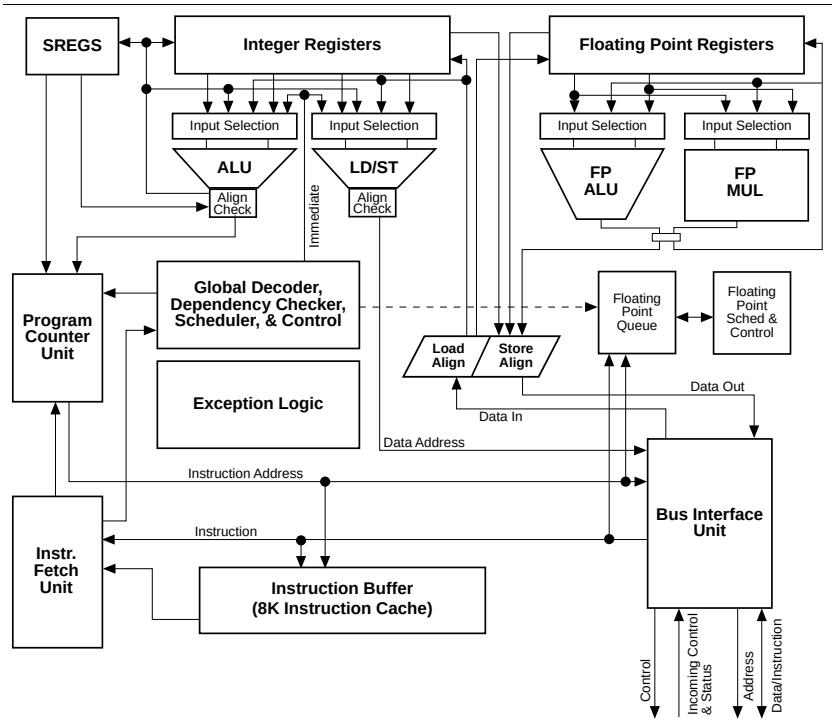

Figure 2. Internal block diagram of the Pinnacle-1 processor chip.

CPU Microarchitecture

Figure 2 shows an internal block diagram of the processor chip. It is a two-issue superscalar design with a six-stage pipeline: fetch, decode, execute1, execute 2, execute 3, and update. There are five parallel execution units: integer ALU, load/store unit, branch unit, FP ALU, and FP multiplier.

There are no arbitrary restrictions on the issue capabilities, such as alignment or instruction placement requirements. Unlike SuperSPARC, however, there is only a single integer ALU, so two integer ALU operations cannot be issued together. Floating-point load, store, and branch are treated as integer operations. The issue logic allows some common instruction pairs to be issued together, even though simple dependency checking would prohibit them. For example, a "sethi" instruction can be issued along with an add/or instruction to form a 32-bit constant, and an add immediate (generating an address for array indexing) followed by a load using the address can be issued as a pair.

The floating-point unit has a four-entry queue, and any two FP instructions can be issued to the queue in the same clock cycle. Instructions can then be dispatched from the queue at a rate of one per cycle, subject to availability of the required execution units.

There is a 64-bit data path from the load/store unit to the floating-point unit, allowing double-precision loads to be completed as quickly as single-precision loads. Single-precision (SP) and double-precision (DP) addition and multiplication are fully pipelined; latency is 3 clock cycles. Divide latency is 10 cycles for SP and 14 cycles for DP; square-root latency is 13 cycles for SP and 19 cycles for DP.

The processor statically predicts conditional branches as taken. An instruction that sets the condition codes can be issued in a pair with a conditional branch, and the processor will then fetch the first pair of instructions at the branch destination. If the condition is true, this pair is issued and there is no branch-taken penalty. If the condition is false (i.e., the branch is not taken), the pair of target instructions is squashed, and execution continues at the next sequential instruction pair with a one-cycle penalty—the same as a 7C601.

Conclusions

The Pinnacle-1 design represents a very different philosophy from the Sun/TI SuperSPARC chip. Instead of using BiCMOS, it uses pure CMOS, and instead of pushing transistor count and die size to their limit, it divides the processor into a set of chips to keep the size of each one relatively modest. Its superscalar capabilities are not as aggressive, but a higher clock rate is expected. Pinnacle-1 supports only two cache sizes and requires four chips for a minimum configuration. SuperSPARC, on the other hand, can be used in a single-chip configuration. Pinnacle-1 has only half as much first-level instruction cache as SuperSPARC, and the lack of an on-chip data cache means that it is one cycle slower on every load or store.

Many observers—especially financial analysts following Cypress' stock—have wondered whether Sun will use Pinnacle-1, given Sun's massive investment in SuperSPARC. While other system vendors may provide some market, Sun remains the only customer that can provide the volume Cypress needs to justify its investment in Pinnacle. If Pinnacle-1 had been ahead of SuperSPARC in reaching production, it might have been able to fill a time gap, but it appears that Pinnacle-1 is well behind SuperSPARC.

Since both SuperSPARC and Pinnacle-1 will be available as MBus modules, with the same physical dimensions and interface connector, it is a simple matter for Sun to support both processors—if there is any reason to do so. New or existing system designs using Cypress' 7C601-based MBus module can be upgraded to either SuperSPARC or Pinnacle-1 simply by changing the processor module and some system-level software. Unless SuperSPARC runs into serious trouble, however, Cypress/Ross will have to price Pinnacle-1 such that it has a compelling price/performance advantage over SuperSPARC to get Sun's business. ♦