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Cyrix Joins x86 Fray with 386/486 Hybrid

Cx486SLC Combines 486-Like Integer Core, 1K Cache, 386SX Pinout

By Brian Case and Michael Slater

Cyrix has made its long-rumored entry into the 386/486 microprocessor market with the Cx486SLC, a chip that combines a 486-like integer core, a 1-Kbyte cache, and a 386SX bus interface and pinout. It does not have an on-chip FPU, but it can be used with Cyrix's (or other) 387-type coprocessors. The 486SLC is aimed primarily at notebook computers, but it will also be used in entry-level desktop systems. A 32-bit-bus version that is pin-compatible with the 386DX is already being sampled, and it will be promoted as a retail upgrade product as well as an OEM product.

Cyrix, a three-year-old, venture-funded startup with 130 employees, produced $60 million in revenue last year from Intel-compatible math coprocessors. It was cofounded by Jerry Rogers, president and CEO, who was formerly head of Texas Instruments' microprocessor division, and by Tom Brightman, VP of systems engineering, who previously worked at TI, Atari, and Commodore. The VP of engineering and head of the chip design team is Kevin McDonough, a former TI Fellow. Jim Chapman, VP of marketing, is a 10-year Intel veteran who most recently served as director of marketing for the 386SX and 386SL. Berry Cash, who was a founder of Mostek and is now a general partner of InterWest Partners III, is chairman of the board. Other board members include L.J. Sevin, also a former Mostek executive and now a partner in Sevin Rosen Management, and Melvin Sharp, an attorney who led TI's intellectual property efforts for over a decade.

On the surface, Cyrix's 486SLC is similar to C&T's Super386, putting a pipelined CPU core and a small cache into a 386-compatible pinout. Cyrix's core is faster than C&T's, however, and its 1K cache is twice as big. Cyrix has priced its chip at 386DX, rather than 386SX, levels, however. The initial version lacks a system-management mode, but Cyrix is now adding this capability to the chip design and expects to have the updated version in production within a few months.

Unlike AMD and C&T, which found their first processor customers in the Far East, Cyrix plans to focus on the leading U.S. PC makers. So far, Tandon, Zeos, and Western Digital have revealed plans to use the Cyrix chip; WD plans to market its system through resellers such as CompuAdd. The Tandon and Zeos machines are both entry-level desktops, while the WD design is a notebook. MicroSlate, a Canadian maker of pen-based systems, also announced plans to use the chip.

Compaq is rumored to be planning to use the Cyrix chip. One of Cyrix's major backers is the Sevin Rosen Management venture capital firm, and Ben Rosen is the Chairman of Compaq, so Cyrix has an exceptional connection there.

While the Cyrix chip will put pressure on Intel's prices, its biggest effect is likely to be on AMD and C&T. Many companies that have invested in designs using

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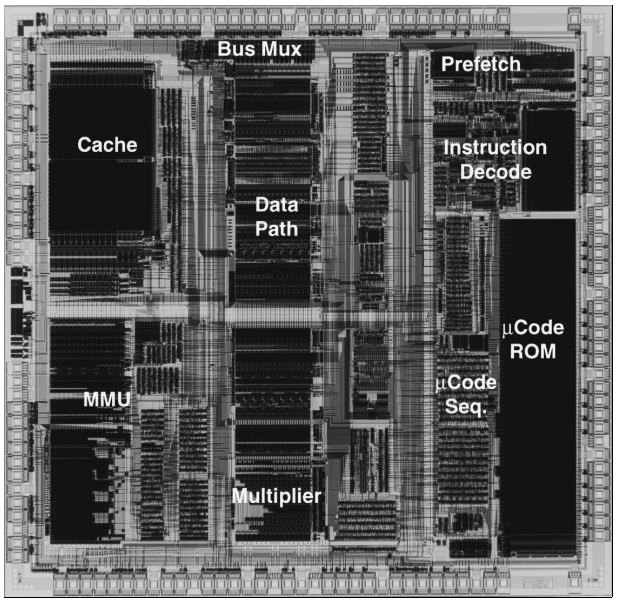
Intel's 386SL may wait for Intel's 486SL (code-named H4C), but companies that have remained with the 386SX will have to consider the Cyrix or C&T chip to remain performance-competitive. IBM's use of its own 386SLC (which is unrelated to Cyrix's 486SLC, despite the similarity in the name) further increases this pressure, since the IBM part offers higher performance than Intel's 386SX.

AMD's customers are, by definition, willing to consider a source other than Intel, and the Cyrix part will give them a significant performance boost. For a company now making a 386SX-based computer, the 486SLC enables them to produce a significantly faster machine with only minor redesign and a processor cost increase of perhaps $40. C&T's Super38605SX makes a similar promise and at a lower price, but the Cyrix part appears to be somewhat faster. The fact that Cyrix had several major U.S. vendors announcing plans to use the part within days of the chip's announcement, while C&T still has no significant announced U.S. customers more than six months after its introduction, indicates Cyrix's stronger position.



Die photo of Cyrix's 486SLC, which includes 600,000 transistors on a 410 x 410 mil (10.4 x 10.4 mm) die.

While AMD has designed its 386 by matching Intel's design very closely and making parametric improvements (such as a higher clock rate), Cyrix and C&T have designed completely new processor cores. This makes the burden of proof with respect to compatibility somewhat greater, but it also allows the products to achieve higher performance levels than Intel's 386. AMD's approach may have been best for the first non-Intel 386 chip, when customers were just getting accustomed to the idea of a supplier other than Intel and skepticism about compatibility was high. As C&T and Cyrix demonstrate their compatibility and the market gets used to idea of multiple implementations of x86 CPU cores, however, AMD will be put in an increasingly difficult position.

Cyrix has created a minor controversy by using the 486 designation for a chip that fits in a 386SX socket, and Intel was quick to attack the device as not being a true 486. From a hardware designer's perspective, Intel is right—the chip certainly does not use a 486 bus interface or have as large a cache, and systems using it cannot be upgraded with Intel's clock-doubler "OverDrive" processors. It can be used with a 387-type FPU, which provides a much smaller and less-expensive alternative to the 487SX, but it does not provide 486-level floating-point performance.

From a software perspective, however, it is a 486—it implements the few new instructions in the 486, and the integer CPU core is similar to that in the 486. From a hardware perspective, "turbo-386SX" is more descriptive, but the marketing value of "486SLC" is far greater—the name prompts users to think of the chip as an entry-level competitor to the 486.

Intel wasted no time filing a patent infringement suit against Cyrix. Even before Cyrix's formal announcement, Intel filed a new suit that is similar to the one it filed last month against Chips and Technologies (see µPR 3/25/92, p. 11), claiming the Cx486SLC infringes four of the five patents asserted against C&T's Super386. In the C&T case, Intel asked for a temporary restraining order, which was denied; in the Cyrix suit, no TRO is sought. Intel's quick action in filing this suit is indicative of the degree to which Intel feels threatened by the part.

Intel conceded that it filed the suit without having examined the Cyrix chip, basing its claim on the assertion that any compatible device infringes its patents. Cyrix is using essentially the same defense as C&T, claiming that its part does not infringe Intel's patents but that, in any case, they are manufactured by a foundry that has a patent cross-license agreement with Intel. (See last issue's article on the C&T suit for details on the foundry license debate.) Cyrix is using SGS-Thomson as its initial foundry, and it is also rumored to be planning to use Texas Instruments—the same foundry C&T is using. There have also been rumors that TI will sell the part under its own name or offer it as a megacell library function.

Just before Intel filed its suit, Cyrix filed suit against Intel seeking a declaratory judgment that its chips were licensed because of the foundry's license. The foundry licensing issue has already been litigated with regard to Cyrix's math coprocessors; a trial was held in January, and a ruling is expected shortly. A favorable ruling for Cyrix would apply equally to the 486SLC, but Intel is sure to appeal.

Chip Overview

The 486SLC is implemented in a 0.8 micron CMOS technology and integrates about 600,000 transistors on a 410 × 410 mil die (about 168,000 mils^2). This is about 65% of the size of Intel's original 1-micron 486 design (which is 256,000 mils^2), which Intel still uses for versions up through 33 MHz, but it is 30% larger than Intel's 0.8-micron, three-level-metal 486 implementation (which is 128,000 mils^2). The larger die size of the Cyrix chip, despite its lack of an FPU and its much smaller on-chip cache, is due to its use of a two-level-metal process and a less compacted design. Fortunately for Cyrix, the profit margins on 386 and 486 processors are still high enough that minimum die size is not critical.

Cyrix has been sampling its first silicon (called the A-0 version). The A-0 silicon has been successfully tested using DOS, Windows, and UNIX environments—an impressive accomplishment for the first silicon of such a device. Cyrix says only three minor compatibility problems have been detected: the STI instruction does not guarantee that the following instruction is executed before interrupts are enabled, interrupts are not always handled properly during the REP MOVS (string move) instruction when in real mode, and there is a problem with single-stepping the HLT instruction. Cyrix has implemented metal-mask fixes for all three problems, and the corrected "A-1" version is now in fabrication. The B-0 version, which is expected to be sampled in July, adds system management mode.

As shown in the block diagram in Figure 1, the major functional logic blocks of the 486SLC are the microcode ROM, the 16-byte instruction queue, the five-stage execution pipeline, the TLB, a two-entry write buffer, and a 1-Kbyte combined cache. Internal data paths are 32 bits wide. The decode logic processes four bytes from the instruction stream each cycle regardless of instruction boundaries.

The most unusual execution resource in the 486SLC is the hardware multiplier, which produces a 32-bit result from two 16-bit operands. The multiplier produces a 16 × 16 result in only 3 clock cycles, as compared to 12 to 25 cycles for a 386SX and 13 cycles for a 486. Devoting silicon area to a fast integer multiplier is uncommon in general-purpose microprocessors, but Cyrix claims that it boosts the performance of display drivers and is also valuable for handwriting recognition in pen-based systems. In addition, the fast multiply could enable the chip to be used for some DSP functions.

The five-stage execution pipeline is very similar to the 486's. The five stages are fetch, decode, micro-ROM access. execute, and register write-back. Intel's 486 has two decode stages, but the micro-ROM access of the 486SLC is essentially a decode function, so these pipelines appear to be nearly identical. In particular, the same branch penalty considerations should apply to each. The 486SLC can execute simple instructions in one cycle, but, as with Intel's 486, additional cycles are required for operand specifiers and instruction prefix bytes. One difference in the resources included in each processor is that the 486SLC does not include a separate address computation ALU, adding one clock cycle to instructions that must compute a memory address.

The package is a 386SX-compatible 100-pin PQFP, but some of the no-connect pins are redefined for power-management and 486-like cache control functions. The extra pins are FLUSH*, KEN*, RPLSET, and RPLVAL* for cache support, SUSP* and SUSPA* for power management, and A20M for address wrap-around control.

Price & Availability

Samples of the Cx486SLC are available now, with production ramping up in May and June. The second stepping, which will add system-management mode, will be available in July. A 33-MHz version is promised for the third quarter.

The Cx486SLC-25 is priced at $119 in quantities of 1000. Pricing in quantities of 10,000 in the third quarter will be under $100. The low-voltage version, the Cx486SLC-V, is priced at $135 at 25 MHz; it is also available in a 20-MHz version for $119 (both prices in thousands).

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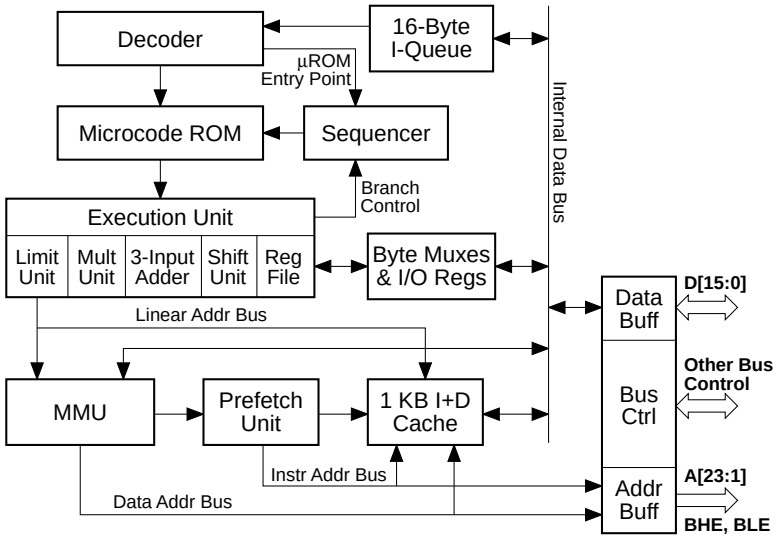

Figure 1. Internal block diagram of the Cyrix 486SLC.

FLUSH* and KEN* are 486-compatible signals. FLUSH* causes the entire contents of the on-chip cache to be invalidated, and KEN* allows external circuitry to control whether or not data being read by the processor is cacheable. RPLSET and RPLVAL*, which are not present on the 486, allow external circuitry to deduce where data is being stored in the internal cache. RPLVAL* indicates that RPLSET is valid while RPLSET indicates which of the two possible lines is being overwritten during a cache-line replacement. These signals are useful for systems with second-level caches that want to track the first-level cache contents.

SUSP* and SUSPA* form a suspend request/acknowledge handshake pair (see power management section).

As in the 486, A20M* allows external circuitry to force the processor to mask address bit 20 for internal cache lookup and external bus writes. The functions of A20M*, FLUSH*, and KEN* are enabled by setting bits in a control register.

The 486SLC's MMU is 486-compatible, except that it is missing the PCD and PWT pins that are intended to communicate per-page cache-disable and write-through status from the TLB to an external cache.

On-Chip Cache

The 486SLC has a rich set of cache and cache-related features. The 1K-byte, combined instruction/data, write-through cache that can be configured under software control for either a two-way set-associative or direct-mapped organization. As with the 486 cache, a write miss does not cause a cache line to be allocated.

The cache has a 4-byte line size with one valid bit per byte. Having a valid bit for every byte costs die size—the tag and valid bit arrays consume as much chip area as the data portion of the cache—but helps improve performance by eliminating the need to fetch an entire line when a cache miss occurs for just a byte or 16-bit word. Since the 486SLC has only a 16-bit bus, requiring a cache miss to fetch an entire line would require two bus cycles instead of just one.

In addition to the KEN* pin and the non-cacheable bits that are part of the 486 page-table structure, the 486SLC provides two other software-determined cacheability controls. Software can set the starting address and size of up to four non-cacheable address regions by writing to control registers. Non-cacheable regions can range in size from 4 Kbytes to 4 Gbytes.

The other cacheability control makes the first 64 Kbytes of every 1 Mbyte region uncacheable. This facility is an alternative to the A20M* pin for solving the problems created by the 8086 artifact of address wrap-around at the 1-Mbyte boundary, and it allows the 486SLC to be used in unmodified 386SX systems that don't provide the A20M* signal. (The wrap-around "feature" is exploited by Microsoft's software to provide an extra 64K bytes of RAM within the real-mode address space.)

One 486 cache feature that is missing in the 486SLC is bus snooping, enabled by the EADS* pin in Intel's 486. This pin allows external bus activity to cause individual cache-line invalidations in the 486 internal cache during periods of bus hold (when the bus is controlled by an external master). To compensate for the absence of this capability, a bit in a 486SLC control register can be set so that the internal cache is completely flushed whenever bus hold is entered. Invalidating individual cache lines with EADS* is important for the 486 because its 8 Kbyte cache is relatively large. Since the 486SLC cache is small, simply flushing it does not cause a huge penalty. Also, bus snooping would have required additional system complexity.

In a typical notebook or low-end desktop system, the only bus-master device other than the processor is the DMA controller, and DMA is typically used only for the floppy disk and, if present, a LAN interface. Memory coherency can be ensured with the 486SLC either by using the automatic cache flush during bus hold, as described above, or by marking the memory areas used for DMA data buffers as non-cacheable. For a Micro Channel or EISA system that could have other bus masters, including a display controller, bus snooping is more important and future high-end chips from Cyrix are likely to implement it.

Power Management

Like the 386 versions from AMD and C&T, the 486SLC uses a static circuit design. While a static design may have a slight negative impact on die size and clock frequency, it allows the processor clock to be stopped, which results in significant power savings.

The 486SLC enters suspend mode in response to the assertion of the SUSP* pin or the execution of a HALT instruction. In either case, SUSPA* is asserted by the processor after pending internal and external activities are completed. External circuitry can then stop the processor's clock.

Suspend mode reduces current drain from 450 mA to 0.5 mA (max. ratings at 25 MHz). By stopping the clock input, current is further reduced by a factor of 10 to 50 μA. For aggressive power-saving designs, the 486SLC will also be available as the 486SLC-V, which operates on a 3-volt power supply. By reducing the supply voltage, current drain is cut to only 225 mA maximum at 25 MHz. In standby mode with the clock stopped, only 10 μA is consumed by the low-voltage part. Unlike AMD's 3.3-V 386 and Intel's 3.3-V 486SX, which have a power supply range of 3.0 to 3.6 V, the Cyrix part has a range of 2.7 to 3.6 V. The 2.7-V specification is significantly harder to achieve, but it is important for some applications because it allows operation

from two penlight batteries.

The system management mode (SMM) functions Cyrix is now adding to the 486SLC are similar to those in AMD's 386SXLV and 386DXLV processors. There are two pins associated with SMM: the system management interrupt (SMI*) and system management address strobe (SMADS*). SMM is activated either by asserting SMI* or by setting the SMM access bit in a control register. The SMI* pin is bidirectional; it is held asserted by the processor when it is in SMM.

SMADS* is asserted by the processor to indicate that the current bus cycle is accessing the SMM address space. The SMM address space is configured by on-chip configuration registers, and it can be from 4 Kbytes to 4 Gbytes. When in SMM, any access to the SMM address space causes SMADS* to be asserted; accesses outside this range cause the normal ADS* to be asserted. SMM accesses are not cached. A bit in a control register allows access to the shadowed main memory while the processor is in SMM.

The SMI* pin also allows trapping of I/O accesses, which is useful to detect accesses to peripherals that power-management software has turned off. If SMI* is asserted at least 3 CLK2 edges before READY* is asserted, then the processor enters SMM and jumps to the SMI interrupt handler. The address of the I/O instruction that caused the trap is pushed on the stack, allowing power-management software to re-execute the instruction after power-management software has turned on the powered-down peripheral.

Performance

Table 1 compares the clock counts for selected instructions in the 386SX, 486SLC, and 486 (SX or DX). While the 486SLC matches 486 performance on the simple instructions that are, of course, the most frequently used, it is not as fast as the 486 on many instructions, even in the case of a cache hit (when its narrower bus is not a limitation). In particular, the 486SLC's lack of a dedicated address adder slows down jumps and calls. There are a few instructions where the 486SLC is faster than Intel's 486, most notably the multiply instructions.

Instruction	386SX	486SLC	486	Comments
Arithmetic and Logical Instructions				
ADD, SUB				
reg.-to-reg.	2	1	1	
mem.-to-reg.	6	3	2	
OR, XOR				
reg.-to-reg.	2	1	1	
mem.-to-reg.	6	3	2	
MUL (acc. w/ reg.)				
multiply byte	12–17	3	13–18	min–max
multiply word	12–25	3	13–26	min–max
multiply dblwd	12–41	7	13–42	min–max
SHL/SHR (shift left/right)				
reg. by 1	3	2	3	
reg. by CL	3	3	3	
CMP				
reg.-to-reg.	2	1	1	
mem.-to-reg.	5	3	2	
String Instructions				
REPNE CMPS	5+9c	5+8c	7+7c	(find match), count > 0
REP MOVS	7+4c	5+4c	12+3c	(move string), count > 1
REPNE SCAS	5+8c	4+5c	7+5c	(scan string), count > 0
STC, CLC	2	1	2	
Control Instructions				
Jump cond.	7+m	6/1	3/1	taken/not taken
JMP (within seg.)				
8-bit	7+m	6	3	
reg. indirect	9+m	6	5	
CALL				
direct in seg.	9+m	7	3	
indirect in seg.	9+m	8	5	
direct interseg.	42+m	30	20	to same level
indirect interseg.	46+m	14	20	to same level
RET				
in seg.	12+m	10	5	
interseg.	36+m	26	18	to same level
LOOP	11+m	9/3	7/6	loop/no-loop
Data Transfer Instructions				
MOV				
reg.-reg.	2	1	1	
mem.-reg.	4	2	1	
POP				
reg. short form	6	3	1	
POPA	40	18	9	(pop all),16-bit/32-bit operands
POPF	5	4	6	(pop flags)
PUSH				
reg. short form	4	2	1	
PUSHA	34	17	11	(push all)
PUSHF	4	2	3	(push flags)

Table 1. Clock cycle counts for selected instructions in Intel's 386SX and 486SX, compared with Cyrix's 486SLC, all in protected mode and assuming cache hits. (m = number of components in target instruction; c = repeat count)

Benchmark	Cyrix 486SLC-25	Intel/AMD 386SX-25	Intel 486SX-25	486SLC % Increase Over 386SX	486SLC % of 486SX
Landmark V2.00	79.44	31.77	80.27	150%	99%
Norton SI V6.0	40.0	12.5	50.6	220%	79%
PC Week	3.62	8.07	3.40	123%	94%
PC Mag. 386 Mix	932	572	1073	63%	87%
PC Mag. FP Mix	305	198	398	54%	77%

Table 2. Cyrix benchmark results comparing an ALR 386SX-25 system with no external cache, the same system with the microprocessor chip changed to a 486SLC, and a Northgate 486SX with 64K bytes of external cache.

Table 2 shows Cyrix's benchmark data, using the most common PC benchmarks. These PC benchmarks are quite small and have high hit rates in the 486SLC's small cache, so while they indicate the peak performance of Cyrix's core, they are not representative of application-level performance. On Norton SI, for example, the 486SLC is rated as 3.2 times the speed of an Intel 386SX, and the PC Magazine 386 instruction mix benchmark rates it at 1.6 times the speed of a 386SX. Both of these figures are exaggerations of the application-level performance boost, which Cyrix estimates to be 40–60% (i.e., 1.4 to 1.6 times the performance of a 386SX at the same clock rate). Cyrix estimates that the 486SLC provides 60–90% of the application-level performance of a 486SX. The 486SX has the advantage of a much larger cache, a slightly faster core, and a 32-bit bus interface.

C&T claims that its 38605SX chip is 40–50% faster than Intel's 386SX, which is in the same ballpark as Cyrix's claims. C&T has not yet provided benchmark data for the SX version of its chip that would enable direct comparison to Cyrix's performance.

Conclusions

The 386/486 microprocessor market now has four vendors and an ever-increasing proliferation of implementations and price/performance points. When Intel was the only vendor, there was a nice, clean price/performance continuum. Now, with several vendors fighting for the same market and striving for differentiation, there is more and more overlap. Over the next year, this situation is going to get even more complex. For system buyers trying to select a computer—and for system makers trying to decide which processors to use—the variety of options will provide more choices, but it will also make the selection process much more difficult.

Better benchmarks are badly needed, as the benchmark results for Cyrix's chip demonstrate; the widely used PC benchmarks are inadequate for gauging the application-level performance differences among microprocessors with differing pipelines, internal caches, and bus structures. One possible answer is an application-based PC benchmark suite that has been developed by BAPCo, a joint venture of Intel and several PC makers, and this suite will be available next month (we'll have details in our next issue).

Cyrix is, in some ways, the most promising of the Intel-compatible microprocessor vendors. The 486SLC provides more differentiation than the AMD processors, and while meaningful comparisons are hard to make with the available data, it appears to be faster than the C&T part. For whatever reason, Cyrix is having much greater success than C&T in signing up U.S. system makers. Texas Instruments' anticipated second-sourcing of the Cyrix chip would firmly establish its designs as a leading alternative to Intel. Cyrix will take some sales from AMD, but AMD has considerable momentum—it shipped about 2 million 386 chips in the first quarter of this year. C&T, however, could find itself in a difficult position in the increasingly crowded and highly competitive 386/486 market, since it has not established much of a foothold.

While Cyrix has introduced only a point product initially, the company has plans for a wide range of devices. While Cyrix could enter the 486 pin-compatible market by providing a version of the 486SLC with a 486 bus interface and a larger on-chip cache, such a device would not be performance-competitive with Intel's 486 unless Cyrix enhanced the CPU core. Cyrix has been in the math coprocessor business for some time, so adding an FPU to the chip should not be fundamentally difficult for them. Their FPU is relatively large, however, so die size could be an issue. Cyrix plans to introduce a superscalar processor in 1993 that it claims will outperform Intel's forthcoming P5, and Cyrix may wait for this core to support the 486 pinout.

The legal cloud remains, and while Intel will surely scare away a few of Cyrix's customers and induce Cyrix to spend many millions of dollars on legal fees, it seems unlikely that Intel will be able to keep Cyrix's products from the market. If Cyrix loses on the foundry licensing issue, it will assert that its chip doesn't violate Intel's patents; if it loses on that issue, it will challenge the patents' validity. Somewhere along the line, it is even possible that an agreement might be reached to license Intel's patents.

Intel's dominance of the PC microprocessor market, which was significantly weakened by AMD and further challenged by C&T, is coming to an end, and PC users will reap the benefits in lower prices and a wider range of price/performance points. In return, PC makers and users will have to cope with a more complex set of alternatives and a more confusing marketplace. ♦