Most Significant Bits

SPARC International Announces V9 Spec

SPARC International has announced the SPARC Version 9 specification, which extends the SPARC architecture to 64 bits and adds several new instructions. This is the first truly collaborative architecture definition, with over a dozen companies participating in the architecture committee that produced the specification. (Sun gave SPARC International responsibility for the evolution of the architecture after Version 8, implemented in the SuperSPARC and hyperSPARC chips, was complete. Version 8 was created by Sun with some collaboration from the semiconductor vendors.)

HaL Computer Systems, a Fujitsu-backed startup led by ex-IBM'er Andy Heller, was a driving force in the creation of the Version 9 specification. In fact, the opportunity to have a major influence on the evolution of the architecture was a key factor in HaL's decision to use SPARC. HaL has announced that it is well along in its implementation of the V9 architecture. HaL will not, however, sell its chips on the merchant market. Other system makers will have to wait for the next-generation SuperSPARC processor from TI or other future SPARC implementations to make use of V9.

At the announcement, a general description of the changes was provided, but copies of the specification have not been made available. The specification will be released in October. (Full details of the architecture will be revealed at the Microprocessor Forum.) The V9 architecture is upward-compatible with V7 (SPARCstation 1 and 2) and V8 (SPARCstation 10) user programs: they will run without modification. The system-level programming model, however, has been changed substantially.

V9 extends all integer registers to 64 bits and supports 64-bit linear virtual addresses. Rather than including a mode bit that would select 32- or 64-bit mode, or requiring a duplicate set of all arithmetic and logical operations for 64-bit calculations, V9 provides two sets of condition codes: one for use by existing 32-bit conditional branch instructions, and one for use by new 64-bit branch instructions. In a few cases, new instructions have been added when the 32- and 64-bit semantics are different (such as for shifts). Instructions for 64-bit multiply and divide have also been added.

In addition to doubling the width of the integer registers, 16 new double-precision floating-point registers have been added, doubling the size of the floating-point register file. These registers can also be accessed as 8 quad-precision registers.

Other user-level instructions that have been added include conditional moves, branches with static prediction, population count, quadword load and store, and speculative loads (cache prefetch hints).

To support multiprocessor systems, an atomic compare-and-swap instruction has been added. A new relaxed memory order has also been added to the memory model, which enables aggressive superscalar processors to allow memory accesses to occur in any order. A memory barrier instruction can be inserted when it is necessary to force ordering.

The system-level programming model has been completely reworked. The PSR has been eliminated, and its former contents divided among several new registers. A hardware trap stack has been added, and there are now five levels of traps instead of just one. Previously, a trap occurring within a trap handler was a fatal event, and trap handlers had to be very carefully coded. With the new programming mode, traps are allowed within trap handlers. According to Sun, this reduces the size of the window overflow trap handler from over 100 instructions to just 19 instructions.

LSI Adds FP to Embedded MIPS Processor

LSI Logic has announced a new version of its LR33000 embedded MIPS processor that includes an on-chip floating-point unit. The new LR33050 is pin-compatible with the LR33000 and is identical except for the addition of the FPU.

LSI joins IDT and Performance Semiconductor in offering such a device, which combines the functions of an R3000 processor, R3010 floating-point accelerator, cache memory, and bus interface logic. Unlike the Performance or IDT parts, LSI's design includes an on-chip DRAM controller and a DMA controller. While any of these chips could theoretically be used in a low-end ARC workstation, LSI developed the 33050 for the embedded market, including PEX (3-D) X terminals, color laser printers, robotics systems, and military applications. RasterOps, which makes a color printer based on the 33000, says that the new 33050 boosted performance by 50%.

Samples are available now at 25 and 33 MHz, with production in the third quarter; a 40-MHz version is promised for August, with production in the fourth quarter. The 25-MHz version in a metal quad flatpack (MQUAD) is priced at $136 in quantities of 1000.

MIPS/SGI Merger Completed

The merger of Silicon Graphics and MIPS Computer Systems was approved by shareholders of both companies, and the chip design and technology licensing operation is now officially the MIPS Technologies, Inc. (MTI) division of Silicon Graphics. All operations are being consolidated at SGI's Mountain View facilities.

In an effort to demonstrate that the MIPS partners will continue to have influence over the evolution of the architecture and its implementations, an executive advisory board has been formed. The board includes Robert Miller and John Hennessy from MIPS; Forest Baskett from Silicon Graphics; Paul Maritz from Microsoft; executives from system makers Acer, Control Data, Olivetti, Pyramid, and Tandem; and executives from semiconductor partners NEC, Performance Semiconductor, Siemens, and Toshiba. Curiously, semiconductor partners LSI Logic and IDT are not represented. Among the system makers, DEC is notably absent.

As part of the merger deal, Silicon Graphics issued 3.6 million new shares of stock, in addition to those traded for MIPS stock. In a show of support for the company and the MIPS architecture, approximately 1.7 million of these shares were purchased by 11 of MIPS' and SGI's technology and marketing partners. Among these are four of the six semiconductor partners: IDT, LSI Logic, NEC, and Toshiba.

P5 Not to be Called the 586?

According to press reports, a strong faction within Intel—led by CEO Andy Grove—does not want to name the P5 the 586. The reason is trademark protection. Intel lost a lawsuit against AMD seeking to protect the name "386," and names following that pattern might not qualify for trademark protection. Intel now uses the names Intel386 and Intel486, and they could do the same by calling the P5 the Intel586. No one other than Intel bothers to use the full name, however, and if Intel calls the chip the Intel586 it will be universally called the 586—a name that others could probably use. Intel is conducting a P5 naming contest among its employees.

DEC apparently jumped the gun on the processor name; a widely-run DEC ad uses the headline "Digital Flight 586 Is Now Boarding" to promote a 486 system that is upgradeable to the P5. The ad claims "the 586 will fit every 400ST Series PC like they were made for each other." (The ad never explains just *how* it is upgradeable, but a salesperson who answered their inquiry line insisted that it was just a matter of plugging in a new chip.)

Intel apparently expressed some displeasure over the use of the 586 designation, and the ad has been changed to replace "586" with "?P5" in all places; a footnote explains that ?P5 is "the yet to be named generation beyond Intel i486." (And yes, the question mark really is there, for some mysterious reason.)

Corollary Shifts MP Chip Set to P5

Corollary has shifted its "SIMPL" multiprocessor chip set plans from 486-based systems to P5-based systems. The chip set, which consists of a cache controller and a data path chip, was first announced 10 months ago (see µPR 8/21/91, p. 1), and samples were originally promised for the first quarter of 1992. Just as the first chip was ready to begin fabrication, however, Intel offered to work with Corollary under non-disclosure, and the company decided to drop the 486 plans and switch to the P5. Samples are promised for November, with production in the first quarter of 1993. One other change in Corollary's plans is that it no longer plans to develop an R4000 version of the chip set, as it originally intended; the company no longer believes that there is sufficient market interest to justify such a development.

Cypress Announces SPARCset Chip Set

Cypress Semiconductor has announced availability of its SPARCset chip set for SPARC-based systems. Cypress claims that the chip set, when used with its 40-MHz 7C601-based processor module, provides 10% to 15% higher performance than a SPARCstation 2. A beta release of Solaris 1.0.1 is available now, and the SunSoft CD-ROM release of Solaris 2.0 due in the third quarter is supposed to provide support for this system design as well as Sun's own systems.

This chip set was designed by Nimbus (see µPR 5/27/92, p. 14), and Nimbus is marketing the same chip set along with a PC board as a complete design kit. Nimbus recently announced a distribution agreement with ASCII Corp. in Japan, which has rights to market the board kit in Japan and Korea.

Cypress will sell the seven-chip set for $250 in quantities of 100. A complete design kit, including schematics, Gerber tapes, layout film, and check plots for the PC board, a bill of materials with alternate sources and costs, and assembly drawings is available for a negotiated fee depending on the quantity of chip sets purchased; for low-volume users, the design kit is priced at about $50,000.

This chip set gives Cypress a complete solution to sell with its SPARCcore modules and its forthcoming hyperSPARC processor, countering an advantage LSI Logic and Fujitsu have had in bundling their processors with their system-logic chip sets.

Toshiba Demonstrates First RDRAM

Toshiba has demonstrated the first complete Rambus DRAM (RDRAM), a 4.5-Mbit device. Until now, only test chips have been shown. Toshiba's demonstration is important both because it shows that RDRAMs are proceeding toward production, and because it helps remove doubts about the ability of the Rambus interface to achieve its aggressive 500 Mbytes/s data rate. Samples are promised for October, with production planned for early '93. Pricing was not released, but Toshiba estimated that the chip would carry a price-per-bit premium of about 25% over a standard 4-Mbit device.♦