Most Significant Bits

Intel Announces DX OverDrive Processors

Intel has announced its clock-doubler OverDrive processors for 486DX systems. These processors are the same silicon as the 486DX2 and the OverDrive processors for SX systems that previously have been announced; what is new is the retail packaging and the certification of many 486DX systems as being upgradeable.

The new OverDrive processors are available for 25and 33-MHz systems. A 25-MHz OverDrive processor is the same as a 486DX2-50, and a 33-MHz OverDrive processor is the same as a 486DX2-66, except that the OverDrive processors come with heat sinks attached and in retail packaging. Intel said that it has no plans for a 50MHz OverDrive processor because of "technological challenges." Intel's "100-MHz" 486, as reported at ISSCC 18 months ago, apparently remains a laboratory curiosity.

The performance increase resulting from an OverDrive upgrade is characterized by Intel as "up to 70%," which is actually conservative—some programs whose critical loops fit entirely in the on-chip cache will speed up by 100%. Intel's OverDrive performance brief (order number 297130-003) shows DOS and Windows application performance increases (in a 25-MHz system) ranging from 33% on AutoCAD display regeneration to 80% on OmniPage386 character recognition.

The OverDrive processors are available in a version that is pin-compatible with the 486DX, allowing existing systems to be upgraded by removing the existing processor and replacing it with an OverDrive processor. Some systems may have problems with such an upgrade for a variety of reasons, however. The OverDrive processors have significantly higher power dissipation, so cooling may be a problem in some systems. They also draw more supply current and have slightly different bus timing (although they meet the 486DX specifications), and these factors may cause problems with some marginal system designs. Finally, a few systems still have speed-sensitive BIOS programs, which may fail with a faster processor.

Intel has conducted an extensive testing campaign and has published a list of systems that have been verified to be compatible. As of press time, 88 models from 52 different vendors have been certified. Intel's warranty is void if an OverDrive processor is used in any system not on the compatibility list.

In addition to the 168-pin, 486DX-pin-compatible OverDrive processor, Intel also offers a 169-pin, 487SX pin-compatible version. This package has an extra pin for alignment, and it also has an arbitrary pinout change to make it incompatible with the 168-pin version. This version of the chip plugs into the OverDrive socket that is included in many 486SX systems, and which Intel is encouraging system vendors to provide in new 486DX systems as well.

The 33-MHz OverDrive processor carries a list price of $799, and the 25-MHz version is priced at $599. A 16- or 20-MHz version, intended for 486SX systems (since there are few 486DX systems at these clock rates), costs $449. You can get a list of compatible systems by calling (800) 538-3373 and asking for a copy of the "OverDrive Processor Compatibility Data."

Cyrix Beta-Testing Clock-Doubler for 386 Systems

Intel has touted upgradeability using OverDrive processors as an advantage of 486 systems over 386 systems, but Cyrix is developing a similar device for 386 users. Cyrix is currently beta-testing a module that includes its 486DLC processor, a clock-doubler circuit, and additional interface circuitry on a small board that plugs into a 386DX socket.

The 486DLC in the upgrade module operates at twice the speed of the system in which it is installed. Even without a clock doubler, a 486DLC (which is pin-compatible with a 386DX) provides an estimated 40% performance boost because of its 1K on-chip cache and faster CPU core. With the clock doubler, Cyrix estimates the average performance boost to be about 70%.

One difficulty with providing a 386 upgrade processor with on-chip cache is maintaining cache coherency. The 486 processor has extra signals for cache control, but these are lacking in the 386 pinout. Cyrix's 486SLC and DLC have redefined a few of the "no connect" pins on the 386 to perform this function, but these signals are only useful if the system's hardware generates them; in a 386 upgrade situation, these signals aren't present.

The Cyrix 486SLC/DLC processor has a software controlled alternative, however. The chip can be configured, under software control, to inhibit caching in the first 64K of each 1M segment, which avoids the A20 wrap-around problem, and to flush the cache whenever a DMA or bus master device asserts HOLD. This is a brute-force way to ensure coherency, and it reduces the cache performance because of frequent flushes. (In systems that don't have a LAN interface, the floppy controller is usually the only DMA device, so cache flushes aren't usually needed.)

Cyrix officials say that the upgrade module has additional circuitry to implement an improved technique for cache coherency, but they won't disclose the details yet.

The prototype module is being tested at large customer sites with quantities of 16- and 20-MHz 386DX-based systems from Compaq and IBM, and limited volume sales of the module may be made to such customers. For the general market, however, Cyrix is developing a single-chip upgrade processor for 386DX systems that it expects to introduce early next year.

Upgrades for SPARC Systems

Weitek is rumored to be working on a new SPARC processor that would extend the chip-level upgrade concept to workstations. By putting a faster CPU core and some on-chip cache in the same package as the processors used in Sun's SPARCstation 1 and SPARCstation 2 lines, Weitek potentially could sell an upgrade chip to most owners of today's SPARC-based systems. While the installed base of perhaps 500,000 is tiny compared to the tens of millions of potentially upgradeable 386 systems, it represents a very big opportunity within the scale of the SPARC marketplace—especially for Weitek, which has had very limited success selling its SPARC processor. Weitek would not comment on any plans for such a product.

Headland Being Folded Into LSI Logic

In a sign of the increasing difficulty of making any money in the chip-set business, LSI Logic has absorbed its Headland Technology subsidiary. Headland's former products will be sold by LSI, cutting the overhead of running a separate operation. Some Headland employees have left the company, and the remainder will be relocated from Headland's Fremont facility to LSI's main plant in Milpitas. LSI plans to focus its system-logic chip set efforts on high-end 486 systems and portable systems.

Headland was formed in 1989 by the merger of G-2, LSI's original chip-set subsidiary, and Video 7, a graphics chip and board maker acquired by LSI. The Video 7 board-level products group was sold last month.

Intel Ships Banding Printer Coprocessor

Intel has begun shipping the 82961KD printer coprocessor, which is designed to work with Intel's 960KA/KB microprocessors in printer controllers. The coprocessor was designed by Peerless Systems (Redondo Beach, CA), a supplier of printer controller technology. The 82961KD is the second chip to result from the Intel/Peerless collaboration; the first device, the 82961KA, was a simpler glue-logic chip designed to reduce the chip count and cost of 960-based laser printers.

The 82961KD includes the glue-logic functions of the earlier device, but it goes much further by providing a coprocessor for rendering display lists into bit maps in real time. In a 960/961KD system, the 960 processor interprets the Postscript or PCL page description language (PDL) and produces a display-list representation of the page. This display list is much more compact and more easily generated than the full bit map. The 961KD coprocessor then renders the display list to create the bit map.

The 961KD coprocessor uses a technique called banding to dramatically reduce the bit-map memory requirements, especially for high-resolution and large-format printers. In a traditional printer controller, the controller must have enough memory to store the bit map for an entire page. This allows the controller to take as long as needed to render the PDL into the bit map. When the bit map is complete, it is a simple task to output the bits to the print engine. This process must occur at a fixed rate, set by the speed at which the printer's drum rotates.

In a banding printer, the full page is interpreted to a display list, but the display list is rendered into a bit map only one horizontal stripe, or band, at a time. This slashes the amount of bit-map memory needed, but it requires that the controller be able to render the display list (for a worst-case page) into the bit map at the rate required by the print engine (7.5 seconds for a full page, for an 8 page per-minute engine). This is not possible with software based rendering using a conventional processor, but the specialized, parallel logic in the 961KD coprocessor is able to render the display list at up to 40 pages per minute.

Banding is often used in printers based on HPs PCL, but it has been limited in its effectiveness. Because the controllers in these printers cannot render complex graphics at engine speed, they can print only text and limited graphics.

The first printer to use Intel's 961KD coprocessor is CalComp's CCL 600, a 600 dpi, 11" × 17" printer priced at only $4495. This printer uses the new Canon BX engine, which is spurring an onslaught of 600 dpi, 11"× 17" printers.

Because CalComp's printer uses the banding technique, it requires only 2 Mbytes of RAM, as compared to over 8 Mbytes for a full bit map of this size and resolution. As printers move to color and higher resolutions, banding will become even more important; an 11" × 17" page at 1200 dpi requires over 32 Mbytes of RAM without banding—and that is for monochrome. A color printer would require up to 24 times as much memory.

The 82961KD printer coprocessor sells for $51.70 in quantities of 1,000 (for the 16-MHz version). Samples are available now, with production in the fourth quarter. Complete printer controller boards (or software and board designs) for Canon's new BX engine or its NX 17-ppm engine are available from Peerless.

Vadem Adds "Ink" Support to Single-Chip PC

Vadem (San Jose, CA) has added a hardware "ink plane" to the LCD controller in revision 2.0 of its VG-230 singlechip PC *(see **0608MSB.PDF**)*. "Ink" is the trail of pixels left by drawing in a pen-based system. Without an ink plane, software must "or" the ink bits into the underlying image. The separate ink plane eliminates the need to manipulate the main display bit map to add the ink bits, significantly speeding up the operation. This is important for enabling the ink to keep up with the pen, especially in a system with a modest-performance processor, such as the V30-based VG-230. The chip is priced at $38 in quantities of 10,000. Samples are available now, with production planned for October. ♦

