ARM250 Integrates RISC System on a Chip

Chip Includes ARM CPU Core with Memory, Video and I/O Controllers

By Linley Gwennap

Advanced RISC Machines (ARM), originally a design group at Acorn Computer, was spun off when Apple decided to use the ARM architecture in a line of portable computers code-named "Newton". The first Newton product will use the ARM610, which is similar to the ARM600 chip presented at last year's Microprocessor Forum (see µPR 12/18/91, p. 8). With Newton still on the drawing board, ARM's biggest customer continues to be Acorn, which sells ARM-based personal computers in the UK education market. At this year's conference, Mike Muller described a new chip, the ARM250, destined for Acorn's product line.

The ARM250 combines the core ARM CPU with a memory controller, video controller, and I/O interface on a single low-cost chip. The addition of DRAM and ROM makes a complete minimal system, and a second chip to connect to a floppy disk and other I/O produces a complete personal computer. The chip shows the flexibility and integration levels possible with ARM's modular design method, but with no cache and limited memory support, this particular chip is not suitable for Newton.

Figure 1 shows a block diagram of the ARM250. The four major functional blocks already existed as discrete parts in the ARM family. The CPU is a slightly-modified version of the ARM2 core called the ARM2aS. The MEMC, VIDC, and IOC blocks are based on a system chip set originally designed at Acorn. The IOC chip was extended by adding the IOEB to decouple the I/O bus timing from the memory system.

The new core is largely code compatible with the ARM2, with a few exceptions. ARM2aS implements a swap instruction (SWP); this instruction causes an undefined instruction trap on previous versions of ARM. Mode changes have been improved so that bank registers can be accessed immediately after the change. Unlike the ARM610, the new core supports only little-endian data, and 32-bit addressing is not included. Although the ARM2aS includes a coprocessor interface, it is not brought out to the pins on the ARM250.

General-Purpose I/O

The IOC provides a simple 8-bit I/O bus by latching data for the main 32-bit data bus. Read data is taken from the low byte, while write data goes to the high byte. The I/O bus can be extended to 16 bits by adding two external latches on the middle bytes of the main data bus. The latching mechanism, along with logic in the IOEB, allows the I/O bus to be clocked at a lower frequency than the main bus. It also allows video refresh cycles to use the main bus during an I/O access, which can be arbitrarily long.

All I/O accesses are memory mapped into the upper quadrant of the 26-bit address space. The "decode" lines from the IOEB can individually select one of six devices; additional devices can be controlled using external decoding logic. The IOEB provides a variety of I/O timing

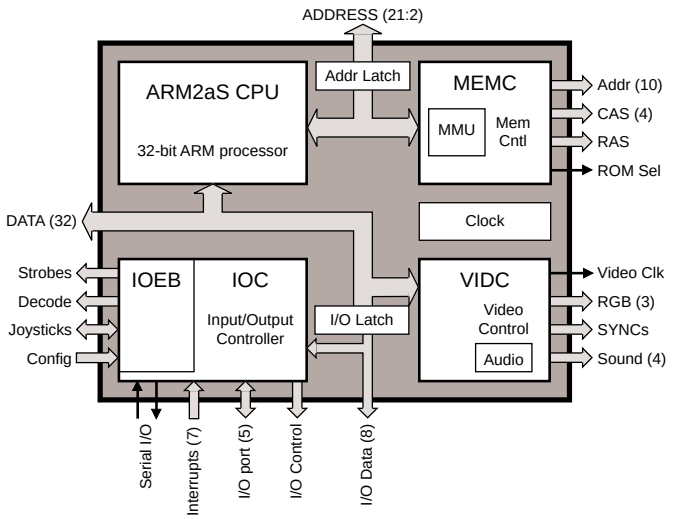

Figure 1. ARM250 internal block diagram.

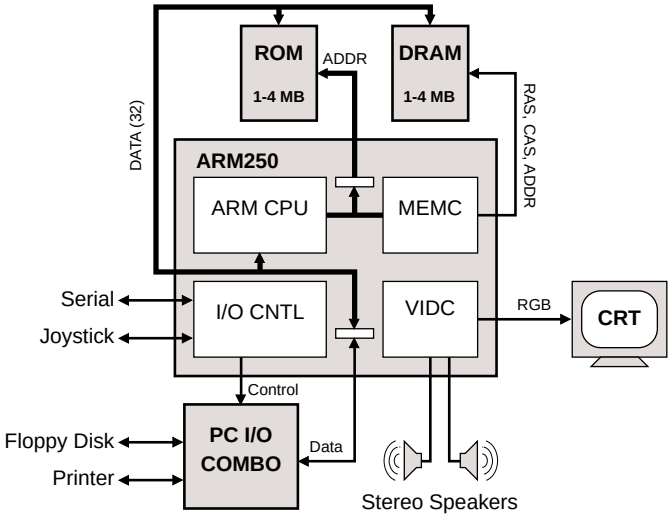

Figure 2. ARM250 low-cost system.

options for each device. According to Muller, one configuration can provide an interface similar to the PC/XT bus.

The IOC includes a serial port that can run asynchronously up to 31,250 bits per second. Three 16-bit timers are available, which are clocked at 2 MHz. Two can be used for general purposes and can generate timed interrupts. The third generates the clock for the serial port.

The IOC also handles all external interrupts. There are seven interrupt signals, most of which are active low with one active high and one edge sensitive. Since the CPU has separate trap vectors for "fast" and "slow" interrupts (see μPR 12/18/91, p. 11), three of the pins produce slow interrupts, two produce fast interrupts, and the other two are programmable for either mode. Any interrupt can be masked by writing to an IOC register.

The chip includes five general-purpose I/O pins. One is internally connected to one of the seven interrupt lines, allowing the interrupt signal to be read at any time; the interrupt must be disabled to use the pin for I/O. The I/O pins are accessed through a register in the IOC. In addition, the IOEB has four configuration pins that can be hardwired or used as status inputs.

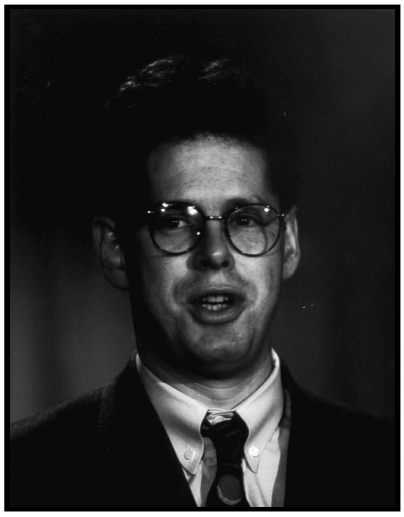

PHOTO BY ANNE HAMERSKY

"This presentation is really an example of a particular product we made for a particular customer. If this happens to be the product that you want to buy, that's fine. If it's not, we can do variants of it...without the usual very very high development costs."

Mike Muller, ARM Ltd.

Audio and Video Features

The VIDC connects directly to a CRT display, as shown in Figure 2, producing RGB outputs and video clock signals. Three 4-bit video DACs create a palette of 4096 colors, up to 256 of which can be used at once. The video controller supports 1, 2, and 4 bits per pixel as well. Both 800 × 600 and 640 × 480 display sizes are supported, along with other smaller sizes. The video output timing is programmable for a range of displays.

Unlike DOS PCs, the ARM250 does not keep the screen image in a separate video memory; it simply allocates a block of the DRAM main memory. The VIDC accesses the screen image using a DMA channel in the MEMC. Screen accesses read 16 bytes at a time to take advantage of page-mode DRAMs and reduce the impact on the system data bus. Although this design allows the CPU to quickly and easily write to the screen, all screen refresh activity will conflict with program instruction and data reads, reducing overall performance. This design does reduce cost by eliminating the external video memory and all of the pins needed to connect to it.

The VIDC provides a hardware cursor, which is a popular feature in graphics accelerators. The hardware cursor is a separate image that can be up to 32 pixels wide and any number of pixels tall. It can use up to three colors, one of which can be "transparent." The software simply specifies the X-Y position of the cursor and the VIDC automatically merges it with the rest of the screen image. The flexibility of the VIDC's implementation means that this feature could be used as a cursor or to display a figure in a video game, for example.

The VIDC also contains an eight-bit audio DAC with eight individually programmable channels. These logical channels are mapped to two stereo output channels. Each logical channel can appear in a separate stereo position using a programmable stereo image table.

Memory Interface and MMU

As shown in Figure 2, the ARM250 connects directly to DRAM and ROM. Although the chip uses 26-bit addressing internally, only bits 21:2 of the address are brought out to the pins, allowing a maximum of 4M of ROM and 4M of DRAM, typically using four 1M × 8 ROMs and four 1M × 8 DRAMs. The two types of memory are selected using separate signals, and the timing of each may be specified individually. The interface uses fast-page-mode accesses where possible to maximize memory bandwidth.

The MEMC block includes three DMA channels for the video display, the programmable cursor, and the sound subsystem. The screen image and the cursor image are held in two separate buffers in main memory; the location and size of these buffers is set by programming the MEMC. Once these buffers are initialized, data is transferred to the VIDC as needed without intervention from the CPU. For sound output, the programmer can set up any number of sound buffers of any length in memory. The MEMC contains pointers to the current sound buffer as well as the next one; when the current buffer is exhausted, the MEMC immediately begins transferring data from the next buffer (if it is valid) and interrupts the CPU so that it can set up a new sound buffer. All DMA transfers take place in blocks of 16 bytes.

The MEMC block includes a 128-entry MMU that maps physical memory into a 25-bit (32-Mbyte) virtual address space. (The 26th address bit selects internal registers and memory-mapped I/O.) No second-level translation table is used; all physical memory must be mapped through the MMU at all times. With the maximum 4M of DRAM, each MMU entry maps a 32K page. With smaller amounts of memory, page sizes of 16K, 8K,

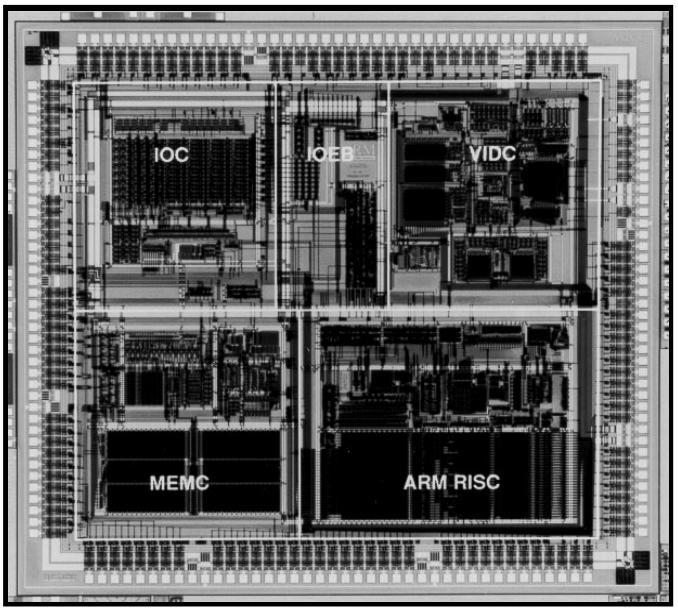

Figure 3. Die photo of the ARM250. The chip uses 98,000 transistors and is 8 mm × 7.2 mm (317 mil × 285 mil).

and 4K are allowed. Three levels of protection are available, but the ARM250 does not provide the ARM610's "domain access" feature that is useful for object-oriented operating systems.

Performance, Power, and Price

The ARM610, with an onboard cache, is rated at 25K Dhrystones, or about 14 VAX MIPS, operating at its peak clock rate of 25 MHz. The ARM250 uses a very similar CPU core but has no on-board cache; all instructions and data are fetched directly from DRAM. With this limitation, the ARM250 typically operates at 12 MHz, or 16 MHz with a fast memory system. According to Muller, at 16 MHz, the chip reaches 14K Dhrystones. Performance on real applications will suffer due to screen refresh accesses.

Unlike the ARM610, the ARM250 has been qualified for operation at 3V. The newer chip uses about 21 mW per MHz at 5V, or 250 mW at 12 MHz. When throttled down to 3V, power consumption goes down to a miserly 90 mW. Although much of the chip is fully static, portions of the IOEB are not, limiting the ability to save power by reducing the clock speed.

This low power consumption is primarily due to the minimal transistor count. The CPU core requires just over 29,000 transistors, and the entire ARM250 uses less than 100,000. The chip is built in a conservative 1.0-micron CMOS process with two layers of metal. The die (see Figure 3) is just 58 mm^2. The ARM250 uses a 160-pin Japanese PQFP (PJQFP).

Advanced RISC Machines does not sell the ARM chips; they are sold through two semiconductor partners, VLSI Technology and GEC Plessey. The ARM250 is available from these vendors at a price of $25 in quantities of 100,000.

Price and Availability

The ARM250 is currently in production. It uses a 160-pin PJQFP and is priced at $25 in quantities of 100,000. Contact VLSI Technology at 1110 Ringwood Court, San Jose, CA 95131; 408/922-5200, fax 408/922-5252. In Europe, contact GEC Plessey Semiconductors at Unit 1, Crompton Road, Groundwell Industrial Estate, Swindon, Wilts SN2 5AF, United Kingdom; +44/793-518510, fax +44/793-518582.

Conclusions

While the ARM250 packs an impressive number of functions into a small space, several design choices limit the usefulness of this particular part. The lack of a cache is a particular hindrance to performance, limiting the instruction rate to the speed of the DRAM. The 4M limit for DRAM is adequate only for low-end systems, although ARM could easily solve this problem by bonding out more address lines. The video controller is adequate for VGA graphics but not for higher color depth or pixel resolution. Separate video memory would improve graphics and CPU performance, particularly in a cacheless system.

The ARM250 was designed primarily for Acorn's personal systems, and it provides an inexpensive solution for such products. The built-in joystick support indicates an interest in the video game market, and it may have some success there as well. The chip may also interest some embedded-application vendors, although the video controller and MMU may not be useful to them.

This product demonstrates the "Quickdesign" concept that differentiates ARM from many other CPU vendors. The company can quickly take existing functional blocks and combine them on a single die to meet precise customer specifications. If the customer doesn't need an MMU, it can be removed. If necessary, cache can be added. As the CPU itself becomes a smaller and smaller portion of the chip, this strategy will be required for most processor vendors to survive.

Apple's selection of the ARM610 has focused ARM on the handheld market. The low power and the affordability of the ARM chips make them well-suited to such applications, but the ARM250 is not the solution for this market. Portable systems need an LCD display instead of a CRT, and some power management capability. ARM is working with Apple and its silicon partners to fill these gaps. Second-generation Newtons will use more highly-integrated ARM chips, similar to the ARM250 but customized for portable products. ♦

