

# At A Glance

## **IBM Delivers First PowerPC Microprocessor.....1**

IBM has built the first PowerPC chips and delivered samples to Apple. The chip uses a modified RSC core with a bus interface similar to the 88110, achieving impressive performance with a relatively small die.

## **RISC's Adjust Course Downward.....3**

Last week's Microprocessor Forum showed that RISC vendors have finally started work on lowering system costs, both in the embedded and general-purpose arenas.

## **Most Significant Bits .....4**

P5 Christened "Pentium"; AMD Plans Intel-Microcode 486; TI announces production of 486SLC and 486DLC; Microchip Technology introduces "mid-range" PIC family; Chips & Technology announces low-power graphics chips; Echelon ships power-line transceivers.

## **SPARC Hits Low End with TI's microSPARC.....11**

Texas Instruments' latest SPARC chip, formerly known as Tsunami, integrates many system functions and enables Sun to build very low-cost workstations, but performance is not impressive.

## **Hobbit Enables Personal Communicators.....15**

AT&T has a complete chip set for building a "personal communicator", including a low-power CPU, system logic, LCD driver, connections to both ISA-type peripherals and PCMCIA cards, and a modem chip set.

## **ARM250 Integrates RISC System on a Chip.....22**

Advanced RISC Machines quickly produced a highly-integrated chip that includes an ARM CPU along with memory, video, and I/O controllers. Similar products could be used in future Apple hand-held devices.

## **Intel Describes P5 Internal Architecture .....25**

At the Microprocessor Forum, Intel revealed new details about the P5 cache configuration and floating point timing. The P5 will also include a set of new reliability features.

## **Recent IC Announcements .....27**

## **Resources .....28**

*Literature Watch will return next issue.*

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