THE EDITOR'S VIEW

RISCs Adjust Course Downward

Lower Cost, Not Higher Performance, is Key to Bigger Markets

By Michael Slater

After several years of single-minded focus on performance, RISC microprocessor vendors have begun to redirect their efforts toward reducing system costs while maintaining or slightly reducing performance levels. This trend is evident in both the embedded and general-purpose arenas.

Vendors have recognized that they have simply overshot the mainstream of the market. Higher volumes will come not from higher performance but from lower costs.

This trend has been evident for some time in microprocessors designed for embedded applications. Over the past 18 months, for example, AMD has added a variety of processors to the 29000 lineup, all of which (except for the 29050) are aimed at cutting system costs. The 29030 introduced a lower-cost bus structure; the 29200 cut out the caches to put system functions on-chip; and the 29xx5 versions are slower, cost-reduced variants. AMD clearly has the technical capability to develop a faster 29000 CPU core, but they haven't bothered because high-volume customers aren't asking for it.

This trend hasn't been lost on Intel either. The 960SA and 960SB are cost-reduced versions of the original 960KA and 960KB with a narrower data bus. Intel hasn't even bothered to market the highest-performance family member, the 960MX, except to a few key military (i.e., price-is-no-object) customers.

IDT has been the most aggressive of the MIPS vendors in bringing the cost of that architecture down, and IDT's most recent entry—the 3041—is a 3051 with smaller caches, no MMU, and a variety of bus changes designed to cut system cost. (We'll have details on the 3041 and several of the other chips mentioned in this article in our next issue.)

Last week's Microprocessor Forum provided clear evidence that this trend has hit the general-purpose RISC market as well. The microSPARC (a.k.a. Tsunami) processor developed by Sun Microsystems and Texas Instruments is the first SPARC processor to focus on lowering costs, rather than increasing performance. It has tiny on-chip caches and an unexciting CPU core, but its on-chip DRAM controller and SBus interface slash the system chip count *(see 061402.PDF for details)*.

Hewlett-Packard is moving in a similar direction. HP revealed at the Forum a new 7100-family PA-RISC chip that includes a small on-chip instruction cache and a DRAM controller. Unlike other recent PA-RISC chips, it has a combined external instruction/data cache. This chip bucks the simplification trend in one respect; unlike Tsunami, which makes no contribution in the CPU core, the new HP device is a more aggressive superscalar implementation than the 7100.

DEC gave a few details at the Forum regarding its future low-cost Alpha (LCA) chip, which echoes the approaches followed by Sun and HP. The LCA chip will include on-chip memory and I/O controllers, be fabricated in a lower-cost process, and use a cheaper package.

The MIPS R4000 architecture is also heading for lower costs. Two efforts are underway to develop lower-cost R4000-class processors, one at MIPS (under contract to NEC), called VRX, and one at QED, called Orion. QED, which is an IDT-funded MIPS spinoff, gave the first preview of Orion at the Forum, revealing that it will cut costs by dropping the on-chip multiprocessor and second-level cache support. Surprisingly, Orion will also use an R3000-style five-stage pipeline, abandoning the R4000's eight-stage superpipeline in return for a simpler design (requiring fewer transistors) and the resulting lower cost.

The Apple/IBM/Motorola PowerPC effort will also have a low-cost thrust. The first device, the PowerPC 601, will be significantly faster than IBM's existing single-chip RIOS processor, but the designers chose to keep the die size modest—a mere 11 mm on a side, tiny by today's high-end RISC standards—rather than pushing the cache size to the limit *(see 061401.PDF)*. This was driven, in part, by Apple's intense focus on low cost. The next device to emerge, the 603, will be *slower* than the 601; the goal is to reduce cost and power consumption even further.

The bottom line is that performance has reached a level that is acceptable for many applications, but costs are still too high for many of them. In the embedded arena, there just aren't any high-volume applications for processors that cost hundreds of dollars, no matter how fast they are. In desktop systems, performance in the 50-SPECmark range will make a lot of people very happy, and most of them would rather see the system cost drop than the performance double. In time, of course, more advanced software will raise the minimum desirable performance level, but this software won't become popular until the faster systems come down to high-volume price points. ♦

