Most Significant Bits

P5 Christened "Pentium"

While many details of the P5 design remain shrouded, one fact has now been announced—the name is "Pentium." As expected, Intel chose not to use the 586 designation because it cannot be protected as a trademark. Intel is sure to invest tens of millions of dollars attempting to create an image for Pentium, and the trademarked name will keep other vendors from directly benefiting from this promotion, as they have from the 386 and 486 promotions. AMD has indicated that it would be happy to call its next-generation chip the 586, regardless of Intel's naming approach. The 586 designation could be used by AMD or others for Pentium-pin-compatible chips, or it might be used for chips that compete in the same performance class but use an extended 486 pinout.

Intel spent a small fortune coming up with the name, but in the end, it won't matter much. Intel likes the fact that Pentium sounds like an element on the periodic table; AMD's Jerry Sanders commented that it sounds like a toothpaste.

AMD Plans Intel-Microcode 486

Bolstered by a ruling from Judge Ingram that upheld the jury verdict in the 287 microcode case but limited its scope to the 287 alone, AMD is reportedly proceeding with plans to enter production with a 486 chip using Intel's microcode. AMD has already demonstrated the device, and volume production is expected by year-end.

While Judge Ingram narrowed the scope of the jury's verdict, he still has not ruled on the key issue of whether the agreement between Intel and AMD gives AMD the right to use Intel's microprocessor microcode. Ingram said that he would rule on this issue, however, and AMD is apparently confident of a positive outcome. Of course, AMD has been surprised in the past. Should Ingram rule against AMD, production would be delayed about six months while AMD completes its clean-room microcode.

TI Announces Production of 486SLC/DLC

Texas Instruments, which revealed last spring that it had licensed Cyrix's 486SLC/DLC processor design, has announced that it is now in production with the 486SLC at 20 and 25 MHz and the 486DLC at 25 and 33 MHz. The 486SLC is pin-compatible with Intel's 386SX, and the 486DLC is pin-compatible with Intel's 386DX *(see µPR 4/15/91, p.1, and* **060801.PDF***)*. Both chips are made from the same die, with only a bonding option and the package type differentiating the two.

TI says that it will introduce its own derivative designs, offering a higher level of system integration, in the first half of next year. TI is a supplier of PC system-logic chip sets, so it has the designs needed to bring these functions on-chip. TI also has a range of DSP cores, including the Mwave processor developed in collaboration with IBM, as well as graphics processors and LAN controllers, but these aren't likely to be the first functions to move on-chip. Such additions would, however, have the advantage of differentiating TI's offerings from Intel's and others. The first derivative designs are likely to be aimed at portable systems, bringing the system logic and perhaps a PCMCIA interface on-chip. Cyrix has some rights to TI-developed derivatives, but TI will be the first to bring them to market.

Cyrix also has a series of new processors in development, including 486-pin-compatible versions and a superscalar competitor to the P5, code-named "Spike." Most, if not all, of the forthcoming Cyrix designs are likely to be produced and marketed by Texas Instruments as well. A TI spokesperson said that their licensing agreement was "multigenerational, but not all-encompassing."

TI is quoting prices considerably below those quoted by Cyrix, but sources indicate that this is a difference in their public pricing strategies, rather than in actual volume pricing. As the table below shows, TI is quoting 1000-piece prices ranging from $59 for the 486SLC-20 to $99 for the 486DLC-33, while Cyrix's quoted pricing is somewhat higher. Actual volume pricing from both companies is rumored to be well under TI's quoted pricing.

Device	Clock (MHz)	TI	Cyrix
486SLC	20	$59	—
	25	$69	$75
	33	$79	$89
486DLC	25	$89	—
	33	$99	$119
	40	—	$149

For Cyrix, having TI in the market is a mixed blessing. Cyrix gains some royalty revenue for chips sold by TI, and TI's endorsement of the chip went a long way in establishing Cyrix's credibility. The fact that the Cyrix-designed chips are being sold by TI provides an absolute assurance that legal squabbles will not take the chips off the market; TI's right to sell chips using Intel's patents is undisputed. TI also may be able to attract customers that would be less likely to deal with tiny Cyrix, especially outside the U.S. where TI has a much stronger presence. On the other hand, TI can be an aggressive competitor, and the presence of two suppliers will force prices down more quickly. One advantage Cyrix has is its ability to bundle the processors with its math coprocessors; for about $20 more than the processor alone, Cyrix will provide the processor and math coprocessor pair.

For comparison, the following table shows Intel's and AMD's fourth-quarter pricing. Prices are shown for 5V versions only, in the least expensive package (PQFP for all except the 486DX-50 and the 486DX2, which are

offered only in a PGA). Intel's volume prices are rumored to be much lower than these official 1000-piece prices, with the 486SX being offered to some customers at prices below Intel's 386DX.

Device	Clock (MHz)	Intel	AMD
386SX	16	$43	—
	20	$53	$37
	25	$67	$43
	33, 40	—	$43
386SL, no cache	16, 20	$45	—
	25	$63	—
386SL	20	$63	—
	25	$86	—
386DX	16–25	$89	$53
	33	$102	$53
	40	—	$53
486SX	16, 20	$94	—
	25	$109	—
	33	$189	—
486DX	25, 33	$317	—
	50	$502	—
486DX2	50	$457	—
	66	$600	—

Microchip Introduces "Mid-Range" PIC Family

Microchip Technology (formerly the semiconductor division of General Instruments) recently introduced a new family of embedded microcontrollers. At the low end, Microchip already has its PIC16C5x family, which is the CMOS version of an earlier NMOS family with a 12-bit instruction format. At the high end, Microchip has its 16-bit PIC17Cxx family *(see **060104.PDF**)*. Now, they have added a new family with 14-bit instructions, the PIC16C6x and PIC16C7x parts. The wider instruction word provides a greater addressing range than the 16C5x.

All of the PIC families implement a Harvard architecture (i.e., separate instruction and data memories). Because of the separation between instructions and data, and because all memory is typically on-chip, the instruction word is not constrained to be a multiple of eight bits. The slight architectural weirdness introduced by the unusual instruction word size is only of concern to developers of software tools; the data paths are 8-bit.

These processors are exceptionally fast for 8-bit microcontrollers. Virtually all instructions execute in 200 ns using a 20-MHz clock. Among conventional 8-bit microcontroller families, only Hitachi's H8 can execute an instruction in 200 ns, and this is true for only a few of the H8's instructions.

The first family member, the PIC16C71, has an 8-level return stack, 36-byte register file, 1K × 14 OTP ROM program memory, 4-channel 8-bit A/D converter (20-µs conversion time), 13 parallel I/O lines, and an 8-bit timer with an 8-bit prescaler. The PIC16C6x parts will be similar, but without the A/D converter. The PIC16C71 is available now, priced at $3.25 in quantities of 10,000.

C&T Announces Low-Power Graphics Chips

Chips and Technologies announced two new chips in its "Vampire" family of low-power graphics controllers. The family now consists of the low-end 65510, a VGA chip for sub-notebook systems; the previously-announced 65520, for low-end notebooks; and the 65530, for high-end notebooks and laptops.

The 65510 is a single-chip VGA solution integrating the controller, clock, and palette. Only a single DRAM is needed for a complete graphics subsystem. The 65510 does not include a DAC, as it supports only monochrome flat panels.

The 65520 and 65530 are pin-compatible and include both a controller and a full RAMDAC. They support up to 512K of DRAM or VRAM. Display options include monochrome and color flat panels and CRTs up to 1024× 768.

All of the Vampire chips can connect to the processor local bus or the 386SL's Peripheral Interface (PI) bus, as well as to ISA, EISA, or Micro Channel. To conserve power, the chips support mixed-mode 3.3V/5V operation, and they offer panel-off and standby modes. Enhanced graphics performance results from a linear frame-buffer design and the (optional) use of VRAM memory.

The 65510, in a 100-pin PQFP, is sampling now and will be in production in November at a price of $20. The 65520 and 65530 are both packaged in 160-pin PQFPs and are in production now. The 65520 is priced at $34 and the 65530 is $41. (All pricing is for quantities of 10,000.)

Echelon Ships Power-Line Transceivers

Filling out its distributed control product line, Echelon has announced power-line transceiver modules for use with its NEURON processor. (Echelon has previously offered only twisted-pair transceivers.) The power-line transceiver is available in two versions. A complete control node, the PLC-10, includes the transceiver, power-line coupling circuit, switching power supply, and a NEURON chip. The PLT-10 module provides just the transceiver. In quantities of 25,000, the PLC-10 is $70 and the PLT-10 is $20.

Transmitting data over the power line at a reasonable data rate with high reliability is difficult, and Echelon developed several advanced techniques for the new transceiver. It uses a spread-spectrum transmission technique to achieve a bandwidth of 10 Kbits/s and forward error correction to compensate for errors. Using 10-byte packets, which are typical for Echelon's control-oriented applications, the throughput is 55 to 60 packets/s. The most common power-line control devices, such as the X-10 system, use a much more primitive technique that has a low data rate and much lower reliability. The X-10 approach is much cheaper, however, and one of Echelon's challenges is to push the home automation industry toward more sophisticated systems that use its increased capability. ♦

