Most Significant Bits

DeskStation Shows Low-Cost R4000 System
Start-up DeskStation Technologies (Lenexa, Kansas) recently previewed the least-expensive R4000-based system yet shown. The system combines the R4000PC processor with an EISA system-logic chip set (from OPTi) and EISA I/O cards.

Aiming to provide better performance than R4000PC systems that lack a secondary cache, but at a lower cost than R4000SC systems, DeskStation's ARCStation 1 uses the R4000PC with a 64-bit-wide, 512K secondary cache controlled by an external cache controller implemented in custom logic. The cost of the external cache controller is significantly less than the price premium for the R4000SC, which uses an expensive 447-pin package and requires a 128-bit-wide cache.

The DeskStation design includes logic to translate the R4000 bus to a 486-type bus for connection to the EISA chip set. This logic is currently implemented in PALs, but it will be converted to a gate array for the production version. The OPTi chip set provides the memory controller and EISA interface, and all the peripherals are connected to the EISA bus. DeskStation developed the "ARCS-BIOS" code, which provides the ROM-based software required to install and boot Windows NT. DeskStation also modified the disk-resident HAL (hardware abstraction layer) to customize Windows NT for use with OPTi chip set and EISA peripherals. The company plans to provide drivers for a variety of popular EISA graphics and disk controller boards.

DeskStation is working with MIPS vendor IDT to make its ASIC and the ARCS-BIOS available to other vendors. This will provide an alternative to the ARCSystem design licensed by MIPS, for which MIPS requires a hefty $500,000 license fee ($1 million if you want source). Compared with the MIPS design, the DeskStation system uses a less-expensive EISA chip set and depends on the chip set for more of the system's functions. Because the memory controller is part of the OPTi chip set, the memory bus is only 32 bits wide; the MIPS design, on the other hand, has a 64-bit-wide memory bus. DeskStation claims that the 32-bit memory does not significantly reduce performance because of the high hit rate of the 512K cache, which is 64 bits wide.

DeskStation is now shipping a developer version of the system, priced at $4995 with 16M RAM, a 200-MB IDE hard drive, a CD-ROM, an EISA SCSI controller, a S3 SuperVGA display controller, and a 15", 1024 × 768 monitor. This price makes it the least expensive R4000 system yet announced. The production version of the system will be announced along with the first end-user release of Windows NT early next year; it is expected to sell for about $5000 without a CD-ROM drive, or under $6000 with a CD-ROM drive. Rather than developing a dealer network, DeskStation plans to market its systems through mail order, with some OEM customers and direct sales to major accounts.

Unfortunately, no Windows NT benchmark results are yet available, so it is difficult to judge how the DeskStation design's performance will compare to other alternatives.

This is only the first of several R4000-based systems that are likely to emerge at PC price points once Windows NT begins shipping. Some vendors hope to reach price points well below the $4995 level targeted by DeskStation. So far, the MIPS reference design (known as the ARCSystem 100, or Jazz) appears to be too expensive to compete at PC prices, so PC developers are looking at adapting PC chip sets (as DeskStation has done) or developing custom chip sets. The only two major PC vendors that have licensed the MIPS design are Olivetti and Acer; while both companies are shipping developer units using the MIPS chip set, Acer is developing its own chip set to reduce costs for the production model.

AMD Expanding Fab in Anticipation of 486...
Undaunted by its loss in the microcode copyright litigation, AMD is pushing ahead with aggressive plans to add capacity for the 486 and other advanced chips. AMD is building a $700-million plant with 60,000 square feet of clean room in Austin, TX. This plant will start out running the 0.7-micron, three-level metal process used by AMD's 486, and the 0.8-micron, two-level metal process for its flash memories. AMD expects that this plant, called Fab 25, will move to 0.5-micron technology and will serve as its production workhorse through the end of the decade.

Fab 25 won't come on line until 1995, however, and AMD's only plant capable of building the 486 until then is its Submicron Development Center (SDC) in Sunnyvale. To meet the near-term needs (which won't be as near-term as AMD hoped, since it must now develop clean-room microcode), a $160 million expansion of the SDC is under way. About 100 employees will be added to the 350-person facility, which is expected to begin producing 486 microprocessors and flash memory in mid-'93. AMD estimates that chips made in the SDC will produce $400 million in annual revenue.

... While Intel Continues Record Spending
When it comes to capital spending, no one in the semiconductor business can match Intel's war chest. Intel claims that it will outspend all other semiconductor companies in 1993—for the third year in a row. Capital spending for 1993 is pegged at $1.6 billion, up 33% from

1992's $1.2 billion budget. R&D spending is projected to be $900 million, up from 1991's $800 million. Intel executive VP Craig Barrett said that Intel will have the capacity to produce 30 million 486 processors in 1993, and that the company's 1995 capacity will be roughly double the 1992 level.

Intel has half a dozen major fab projects under way in 1993. The only new fab, named F10, is being built in Ireland and will run a 0.6-micron process on 8" wafers, with the initial production ramp planned for 1994. Expansions and upgrades will be performed at several facilities, including D2 in Santa Clara, F7 and F9 in New Mexico, F5 in Oregon, and F8 in Israel, all of which will be running 0.8 micron or denser processes. Intel recently opened its most advanced facility, the D1 plant in Oregon, which runs a 0.4-micron process with 8" wafers.

Hitachi Licenses Rambus Interface Technology

Rambus has signed up its fourth semiconductor licensee: Hitachi. The first three licensees—Fujitsu, NEC, and Toshiba—signed up to make Rambus DRAMs (RDRAMs), and all three are expected to ship products in '93. Hitachi will not make RDRAMs, however, at least initially; its main interest is in providing Rambus interface circuits as part of its ASICs. No specific product announcements have been made.

The narrow, high-bandwidth Rambus technology is tantalizing *(see **060303.PDF**)*, but so far only prototype RDRAMs have been shipped and many potential users remain skeptical about what the price premium will be. Getting support from vendors of ASICs and other interface chips is also critical to Rambus' success; Hitachi is the first semiconductor company to publicly join the Rambus bandwagon since the company revealed its technology last March.

IBM to Develop PowerPC Notebook with Tadpole

In an effort to expand the range of PowerPC systems being developed, IBM is working with U.K.-based Tadpole Technology to develop a PowerPC-based laptop that will be sold under the IBM name. Tadpole currently manufactures and markets a SPARC-based laptop. The two companies are currently negotiating an equity investment by IBM that will help fund the development.

LSI Logic and Dolphin to Collaborate on SCI

Hoping to bring the newly standardized Scalable Coherent Interconnect (SCI, also known as IEEE-1596) into widespread use, LSI Logic has licensed from Dolphin SCI (Norway) designs for SCI interface cores. These cores, totaling about 70,000 gates, initially will be available only to customers that combine them with their own bus interfaces and other logic, but standard products will follow soon. Board-level products using SCI ASICs are expected to be on the market by mid-'93, with systems following later in the year.

Dolphin SCI Technology A.S. is a spinoff of Dolphin Server A.S., formerly called Norsk Data. Dolphin's team has been active in SCI since the inception of the IEEE working group. Dolphin is currently using a GaAs implementation of its SCI interface circuits, and both Dolphin and Vitesse are marketing the GaAs chips.

SCI was originally developed with a focus on large multiprocessor systems, and it includes a directory-based cache coherency scheme that does not use snooping and is therefore scalable to larger numbers of processors. In addition to large MP applications, SCI is expected to find applications as a high-speed LAN replacement for computing clusters and as a computer-to-peripheral interconnect for very high bandwidth devices, such as high-resolution video systems.

SCI uses point-to-point interconnects with a ring topology. Individual links can be implemented using either serial or parallel connections. Dolphin's GaAs implementation achieves a data rate of 1 Gbyte/s; serial connections using fiber links currently run at 1 Gbit/s. Using LSI's core technology, an SCI ASIC can be built to connect directly to a 10-meter cable, providing a 16-bit parallel interface. LSI has not committed to a specific data rate, but it is expected to perform at a minimum of 125 Mbytes/s.

Intel Announces Open Licensing of PCI Patents

In a refreshingly out-of-character action, Intel has announced that it will provide no-cost licenses to any PCI-related claims in patents that may be issued on its technology. The PCI (Peripheral Component Interconnect) bus *(see **060902.PDF** and **061602.PDF**)* was developed by Intel but is being promoted as an industry standard. It has widespread support from major system makers, chip-set makers, and suppliers of peripheral chips such as LAN and SCSI controllers. Intel has turned the administration of the specification over to an independent PCI Special Interest Group (SIG).

One concern that has recently been raised is that Intel might use its pending patents on PCI technology to collect royalties from chip and system makers after they had made significant investments in the technology. Intel made the unusual announcement of open licensing to squelch any such rumors. In a sharp departure from its approach with its x86-related patents, Intel has decided to encourage standardization by eliminating the barrier represented by the patents, instead of trying to corner the market for PCI technology or extract royalties from competitive suppliers. For PCI to be successful, Intel must overcome vendors' resistance to another "open" Intel standard, and clearing up the patent issue is a good start. ♦

