MacroTek to Sell VME Chip Set for PowerPC

German Start-Up Markets Two-Chip Set for System Logic

By Linley Gwennap

MacroTek is developing the first commercial system-logic chip set for the PowerPC family. Its HiBRIC (High-Bandwidth Resource Interface Controller) chip set provides memory control for up to two PowerPC processors along with a VME bus interface. The design uses some interesting technology to improve system-level performance, but its high price tag ($350) and use of VME will keep it out of high-volume PC designs. VME does have an installed base of more than a million systems, mainly in embedded applications; the MacroTek chip set can bring the performance of PowerPC to these systems.

The start-up company plans to sample HiBRIC in 4Q93 and expects to be the first to market a system-logic chip set for PowerPC. It got a head start by using a chip set originally intended for the 88110. Since the PowerPC 601 bus interface is very similar, it was fairly simple to adapt the chip set to the 601.

Chip Set Overview

HiBRIC is a compact solution for VME systems using the PowerPC 601 chip *(see **061401.PDF**)*. MacroTek's chip set will also support the forthcoming PowerPC 604, which is expected to double the performance of the 601 in a similar package, and the lower-cost PowerPC 603.

HiBRIC uses two chips, both of which connect directly to the 64-bit processor bus, as shown in Figure 1. The MEM chip controls up to 2G of DRAM. The VME chip connects to a standard VME bus and also provides control signals for a 68040-like processor bus. HiBRIC allows for an optional second processor without any additional logic. The chip set supports split transactions with out-of-order completion, as defined by the 601 processor bus.

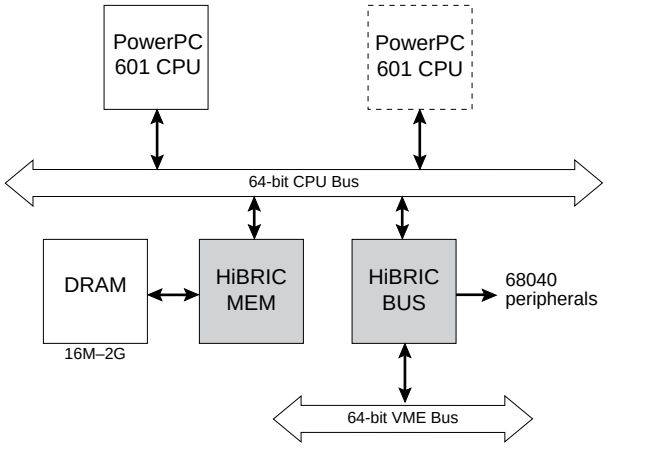

Figure 1. MacroTek's HiBRIC chip set provides DRAM control and a VME bus interface for the PowerPC 601 processor.

The memory controller uses a 128-bit DRAM interface with an additional 12 bits of ECC (error-correction codes). Data is interleaved on page boundaries to improve performance. Given the wide interface, the minimum memory size is 16M, and memory can be added only in 16M increments.

The DRAM timing is configurable. With 60-ns page-mode DRAMs, the first 8 bytes of data are returned to the processor in 7 cycles, with the subsequent data on each of the next cycles (7-1-1-1 pattern) with a 50-MHz processor. With a full-speed 66-MHz 601, the data pattern is 8-1-2-1 with 60-ns DRAMs.

Memory Look-Ahead

To reduce the effective memory latency, the MEM chip uses a look-ahead mechanism that MacroTek calls "streams." The chip has eight 32-byte buffers that each hold a single cache line. Whenever a request is received, the fully-associative stream tags are checked to see if the data is already buffered. If there is a hit, the data can be returned to the processor in a 4-1-1-1 pattern. On a hit, MEM also immediately begins to fetch the next sequential cache line from DRAM.

If the requested information is not present in any of the stream buffers, it is fetched from main memory. Once that access completes, the chip reads the next sequential cache line as well. This data is stored in the least-recently used stream buffer in hopes that it will be needed soon. This simple algorithm can fetch data before it is requested, overlapping the memory latency with code execution. It can also increase the effective memory bandwidth by taking better advantage of page-mode accesses.

The eight buffers can be configured for code only, data only, or split evenly between code and data. With eight code buffers, the chip can maintain a high hit rate across several levels of subroutine calls. In code with very poor locality, however, the look-ahead accesses can conflict with processor requests and reduce overall performance; in these cases, streaming can be disabled or set to only fetch lines that have a prefetch "hint" from the CPU. Using the buffers for data can improve performance for programs that use large data arrays or perform long block transfers on VME.

MEM contains a four-channel DMA engine and four programmable timers. It can also be connected to one

Price and Availability

Each of the chips in the HiBRIC chip set use a 456-contact DTAB package (see text). MacroTek plans to sample the two-chip set in 4Q93 with volume shipments in 1Q94. The company quotes a price of $350 at 50 MHz or $420 at 66 MHz, both in quantities of 1000.

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bank each of ROM and SRAM. The optional SRAM acts as fast memory, not as a secondary processor cache; an external cache controller is required for a second-level cache, since the PowerPC 601 does not include this feature. The address range and data widths for the ROM and SRAM are programmable. For devices less than 128 bits wide, parity is supported instead of ECC.

VME Interface

The VME chip implements a 64-bit VME bus interface according to VME revision D, with a typical bandwidth of about 120 Mbytes/s in synchronous mode and 16 Mbytes/s operating asynchronously. The chip can be both a master and a slave on the bus. It includes a full VME bus arbiter. The chip also translates up to 48 VME interrupts into PowerPC interrupts using four programmable priority levels.

Since the CMOS chip cannot directly source and sink the high-current signals needed to connect to VME devices, it requires external buffers. The chip provides the necessary control signals for these buffers.

The VME chip also provides control signals for a 68040-like local bus. This bus can be used for standard '040 peripheral chips. Address and data lines for this bus are multiplexed onto the same pins as VME address and data; since these signals are already buffered, no additional logic is needed to create the local peripheral bus. This interface adds only 12 control signals and 12 more interrupt lines to the chip.

Demountable TAB Package

Both chips are packaged using DTAB (demountable tape automated bonding) technology developed by Hewlett-Packard. Standard TAB packaging is becoming more commonplace; TI's microSPARC is the first popular microprocessor to use this method. While a standard TAB package is soldered to the board, DTAB uses a mechanical screw-and-plate system to align the package and create a pressure contact between the tape and the board. The advantage is that the chip can be easily removed by simply undoing the screws.

DTAB (or TAB) is about the same price as a ceramic PGA and can handle an equivalent number of signals. Since the die is mounted face down, the heat sink can be bonded directly to the back of the die, improving cooling efficiency. Most importantly, the tape interconnect creates a "smoother" electrical environment than the pad-to-wire-to-pin-to-board connections in a PGA, allowing higher operating frequencies.

The HiBRIC chips use a package with 456 contacts on a 60-mil spacing. The package itself is 5-cm square and 0.5-cm high (without the heat sink). The chips dissipate about 10 watts combined at 50 MHz.

Other PowerPC Chip Sets

Motorola confirmed that it is developing system-logic chip sets for its PowerPC processors but would not provide any specific details of these future products. Motorola is focused on the PC market and will sell chip sets that connect to popular PC buses, including PCI. The first product is expected to sample in 1H94 and will be competitive in price and feature set to Intel's PCIset for Pentium *(see **070403.PDF**)*. Since this is the same schedule as the low-cost PowerPC 603, the chip set may target this processor rather than the 601.

Motorola also believes that PowerPC chip sets will be available from third-party vendors that are currently supplying x86 PC chip sets. These unnamed vendors might license the Motorola design or might produce their own designs. The company expects that some announcements in this regard will be made by Fall Comdex, but the third-party products would not be available until 1994.

IBM's Technology Products Group is developing a system-logic chip set for PowerPC, but the company would not reveal any details or schedule for delivering this chip set.

Conclusion

The HiBRIC design uses some interesting innovations to offer enough memory performance to match the needs of up to two PowerPC processors. In particular, the "stream" buffers are unusual for a standard system-logic product. DTAB packaging keeps the cost down while providing for the large number of interconnects needed for this design.

The use of VME as an expansion bus, while providing adequate performance for many applications, restricts HiBRIC to the embedded market, where VME is most popular. MacroTek points out that its chip set could be adapted to a different expansion bus simply by swapping the VME chip; a PCI adapter is a logical alternative, but the company would not comment on this option.

Motorola continues to aim PowerPC for the PC market and is developing its own system-logic chips (see sidebar). MacroTek's design is best-suited for high-performance systems where VME is a suitable bus and cost is less of an issue. ♦

