Most Significant Bits

IBM Pushes PowerPC into Embedded Market

Continuing its push to become a major merchant microprocessor vendor, IBM's Technology Products Group announced that it plans to market a family of PowerPC processors specifically designed for the embedded controller market. The first chips in the new PowerPC 400 family are expected to sample in 1H94 and sell for $30–$50 in volume. They will be instruction-set compatible with the 601 and other 600-family chips but will use a new core designed by IBM engineers. Currently, Motorola has no plans to second-source the 400-family processors; Motorola is developing its own embedded PowerPC chips for Ford and others *(see **0604MSB.PDF**)*.

IBM expects the new chips to appear in printers, X-terminals, PDAs, and other high-end embedded applications. They will also be used in digital cable set-top boxes through the Scientific Atlanta partnership (see µPR 7/12/93, p. 5). IBM expects that the low-cost PowerPC parts will be used in many IBM products but would not discuss a target ratio for internal consumption versus external sales.

The PowerPC 400 chips will take advantage of IBM's 0.6-micron, four-layer-metal CMOS process to minimize both die size and power dissipation. The company plans to disclose technical details about the new family late this year and announce price and availability early next year.

IBM to Develop RISC-based PCs and AS/400s

Big Blue's RISC processors will be playing a larger role in the company's own products. IBM announced the formation of a new group described as a joint venture between the IBM PC Company and IBM's Advanced Workstation Systems Division (AWSD), which is responsible for the RS/6000 family. The new group's charter is to develop desktop systems similar to IBM's traditional PC products but using PowerPC processors instead of x86 chips. The group will port OS/2 to the PowerPC architecture for use with these systems.

IBM also confirmed that it plans eventually to move its AS/400 customers to RISC-based systems. Current AS/400 systems use proprietary CISC processors. These products have been quite popular, with an installed base of more than 200,000 systems, and have been the top-selling minicomputer family. By using the same processors as the RS/6000 line, IBM will reap considerable savings in development costs while significantly improving performance and price/performance.

The announcements indicate that IBM is adopting the same strategy as rivals HP and DEC, both of which have shifted their products away from proprietary CISC processors and adopted their own RISC standards. The last bastion to fall may be IBM's enormous but faltering mainframe business; AWSD has already announced a 16-processor system that offers performance similar to some of these mainframes.

If IBM can unify its various product lines around its RISC architectures, it could focus tremendous R&D effort on these processors, giving IBM a leg up on lower-volume competitors. Porting OS/400 to its RS/6000 systems would allow IBM to retain much of its AS/400 customer base while virtually eliminating hardware-system development for that product line. The single-architecture strategy has worked well for HP and could be a powerful dose of medicine for IBM. Given the complexity of porting vast amounts of software, however, it will be years before this vision becomes reality.

Intel Attempts to Patent Upgrade Socket

Touching off yet another patent battle, Intel has filed, in several countries, for patents on its "vacancy" strategy. The patent applications relate to the idea of a system with a second, empty processor socket that, when filled by an upgrade processor, disables the original CPU. Since US patent applications are not publicly available, it is not known whether Intel has filed for such a patent in the US, but such an action would fit the pattern.

The proposed patent would apply to systems, not chips, and would cover any system with an "OverDrive" socket; in fact, the claim may be broad enough to apply to non-x86 systems using a similar strategy. If granted, this patent could be used against PC vendors that build motherboards combining non-Intel processors with an OverDrive socket. Given the popularity of these upgrade sockets, PC makers would find it difficult to consider other processor vendors. So far, the upgrade patent has not been approved in any country.

Covering all upgrade paths, Intel has also licensed Acer's patented ChipUp technology that allows 486 systems to be upgraded by replacing the socketed CPU. The patent presumably covers jumpers that enable the upgrade. ChipUp also features copyrighted BIOS code that detects and handles the new processor. Intel's license includes the right to sub-license ChipUp to system vendors, giving Intel another arrow in its patent quiver.

AMD Rumored to Have 50-MHz 486SX2

AMD would not confirm press reports that it has developed a 25/50-MHz clock-doubled 486SX. The chip would be identical to Intel's 486DX2 chips except for the omission of the math coprocessor. Such a product would fill one of the few holes in Intel's product matrix and could offer a grave threat to that company's pricing structure: Intel has maintained a large price differential between

its SX and DX products but has chosen not to offer SX processors faster than 33 MHz, forcing customers to move to the pricier DX chips for better performance.

So far, AMD has chosen not to rock the boat with its 486 product announcements *(see **0709MSB.PDF**)*, keeping its prices in line with Intel's. AMD has little incentive to cut its prices because it is currently able to build 486 chips only in limited volumes. When it is able to increase its manufacturing capacity, probably around the end of this year, weapons such as the 486SX2 could be deployed in an attempt to gain market share.

Intel, ATI Team on Multimedia Standard

Intel and ATI announced a joint effort to simplify the combination of graphics and video in personal computers. The key to this effort is the Shared Frame Buffer Interconnect (SFBI) that allows graphics and video chips to share the same memory and RAMDAC, eliminating many redundant components. The two companies have developed a set of hardware and software definitions for SFBI that they intend to make openly available with no licensing fees.

SFBI is similar to the Media Channel proposal that is currently in the final review process by VESA. Both focus on sharing memory between graphics and video. The VESA proposal is designed to connect separate add-in cards and is limited to 33 MHz; SFBI, on the other hand, is intended to connect multiple chips on a single board and thus can reach speeds of 50 MHz.

Current products such as Oak's Spitfire chip and Tseng's W32 family *(see **070901.PDF**)* are already trying to address this issue. These chips combine video processing and graphics acceleration so the two functions can use the same memory. Both SFBI and Media Channel would go beyond these products by allowing chips from different vendors to share data.

An important issue is software support. VESA says that Media Channel requires no software changes, making it compatible with existing applications. Intel and ATI have developed a new API that they hope will be adopted by Microsoft in its Video for Windows product.

ATI claims that the new API is required to improve performance, and that SFBI is technically superior to Media Channel in other ways as well. Although Intel and ATI are proposing their design as an open standard, they will not make full technical details available until this fall. In the meantime, the partners plan to unveil the first SFBI products, based on an ATI graphics controller and an Intel i750 video chip, at Fall Comdex. Thus, any vendors that license SFBI will be six to twelve months behind the two originators.

As with most standards battles, the deciding factor will be which side can garner the most support. VESA consists of nearly 200 companies that manufacture chips and boards for graphics and video; Intel and ATI are the only companies backing SFBI. The two companies will have to demonstrate clear superiority of their standard for it to succeed against the combined backing of VESA.

Motorola DSP Targets Digital Cellular Phones

As the cellular-telephone world goes digital, Motorola plans to play a major role with its 16-bit DSP chips. Building on the success of its 56156, which is the leading DSP for European GSM digital phones, Motorola announced its new 56166 chip specifically for the emerging US and Japan VSELP-based standards.

GSM (global system for mobile communications) is the digital standard for cellular telephony throughout Europe, Australia, India, and China. BIS, a research firm, projects that sales of GSM phones will hit one million units in 1993, matching the sales of analog cellular phones, and will increase rapidly in the future.

Both the US and Japan have selected a slightly different standard based on the VSELP (vector sum excited linear predictor) compression algorithm. The US standard achieves an 8:1 compression rate, while the Japanese version pushes the rate to 9.5:1. The new digital system recently became active in several major US cities and is planned for a 1994 deployment in Japan. Given the added signal quality, capacity, and security of the digital phones—and their rapid acceptance in Europe—Motorola expects that the market for digital phones will grow quickly in the US and Japan.

Motorola's new 56166 DSP is quite similar to the '156 but has been modified to suit the new standard. In addition to a 16-bit DSP core (common among the 56100 family), the new chip includes 24K of ROM, 8K of RAM, a PLL, 14-bit A/D and D/A converters, and two serial ports. The major changes from the '156 are the doubling of the amount of RAM and the number of serial ports.

The '166 is rated at 30 native MIPS at a clock rate of 60 MHz. Power dissipation is 450 mW at 5V, a 40% reduction from the '156, due to a shrink to a 0.65-micron process and improved circuit design. Despite the increased amount of RAM, the shrink keeps the die size about the same as the older part. The '166 uses a 112-pin PQFP and is available immediately at $60 in quantities of 1000.

Tom Whiteside Takes Over at MIPS

After Bob Miller's departure as president of MIPS Technologies, Inc. *(see **0704MSB.PDF**)*, the company has recruited Tom Whiteside of IBM to take his place. Tom has been an important participant in the development of the POWER architecture and the first RS/6000 systems. He was the first co-director of the joint IBM/Motorola Somerset design center for PowerPC processors. Most recently, he was overseeing the RIOS-2 project and other POWER processors at IBM's workstation division.

In his new role, Tom will be managing the development, marketing, and alliance activities of all MTI

processors, including the R4200, R4400, and the forthcoming T5. He will also help establish future directions for the TFP program *(see **071102.PDF**)*. He will report directly to Wei Yen, chief operating officer of Silicon Graphics.

BAPCo Releases New Benchmarks

The Business Applications Performance Corporation (BAPCo) announced a new benchmark, SYSmark93 for DOS, that is an upgrade to its SYSmark92 test suite *(see **061302.PDF**)*. Like its predecessor, the new suite includes many popular PC applications, such as WordPerfect, Lotus 1-2-3, and dBASE. SYSmark93 for DOS features the latest releases of these programs.

BAPCo also announced a benchmark called SYSmark93 for Windows. As you can guess, this suite consists of popular PC applications for Microsoft Windows. Both SYSmark93 suites are designed to test actual applications performance and exercise the complete system: processor, memory, disk, and graphics. The new test suites are available for $390 each; contact BAPCo at 408/988-7654 (phone) or 408/765-4920 (fax).

Errata: Destiny Address

Our article on Destiny Technology *(see **071001.PDF**)* provides an incorrect address for the company. Contact Destiny at 3255-1 Scott Blvd., Suite 201, Santa Clara, CA 95054. ♦

