Packaging Influences Microprocessor Cost

Ball-Grid Array Could Supplant Current PQFP, PGA Packages

By Linley Gwennap

*This is the third in a series of articles on integrated-circuit manufacturing. The first covered basic manufacturing issues (see **070705.PDF**), while the second discussed cost (see **071004.PDF**). Future articles will discuss more packaging alternatives and compare vendors' IC manufacturing capabilities.*

Most microprocessors today are sold in one of two package types: plastic quad flat packs (PQFP) or ceramic pin-grid arrays (CPGA). Plastic packages keep costs down, but ceramic packages can handle more signals, more heat, and larger die. These two package types cover a wide range of applications. Their characteristics affect the cost and performance of most processors.

In the never-ending search for a better way, many vendors are examining alternative packages. Some of these alternatives are variations of the PQFP. To improve heat dissipation, some are replacing the plastic with metal or ceramic. Another variation, called shrink (or thin) packages, reduce the overall package size. These variations are in production today.

A more radical alternative is the ball-grid array (BGA), which replaces the pins on the package with solder balls. This design can reduce package size and, in some cases, cost, while improving manufacturability. Several processor vendors are currently investigating the use of BGAs, although no merchant market processors using this technology have been announced.

Plastic Packages Prove Popular

According to Integrated Circuit Engineering (ICE), a research firm in Scottsdale, Ariz., plastic packages account for more than 90% of all IC packages consumed worldwide. They are universally used for memory and other commodity chips due to their low manufacturing cost. Most of these chips use some variety of the familiar dual inline package (DIP), which has two rows of pins as shown in Figure 1. Similar, smaller packages are used for surface-mount boards (see sidebar below).

Many microcontrollers, with their 8- or 16-bit designs, are available in DIP packages. Due to their relatively large pin pitch (the spacing of the centers of the pins), DIPs are generally limited to 64 pins. A package of this size is more than three inches long; devices with more pins would be even larger.

Some microcontrollers, and nearly all 32-bit processors, require more I/O signals than a DIP can handle. These chips, and other high-pin-count devices, typically use a PQFP package like the one shown in Figure 1. By arranging pins on all four sides of the package and packing them more tightly, a PQFP can have as many as 304 pins. Most PQFP packages follow the EIAJ standard but some vendors, including Intel, use JEDEC packages with "bumpers" on the corners, also shown in Figure 1.

Plastic packages are popular because of their low cost and high-volume production process. A plastic package starts with a lead frame that carries the signals from the die to the pins, or *leads*. As depicted in Figure 2, lead frames are often produced in groups; five or more is common. A die is placed in the center of each frame and the pads are connected to the frame by heating and attaching fine gold wires. Today, most wire-bonding is performed by machine.

Once the dice are in place, the lead frames are placed in an injection mold and coated with plastic. This step is called "encapsulation." The coated frames are stamped to shape the leads and separate the parts, which are then ready to be tested.

Figure 3 shows cutaway views of various plastic packages. The DIP part's straight pins are long enough to go through a standard PC board, while the PQFP's "gull-wing" leads sit on top of the board. The less-common plastic leaded chip carrier (PLCC) has J-leads that

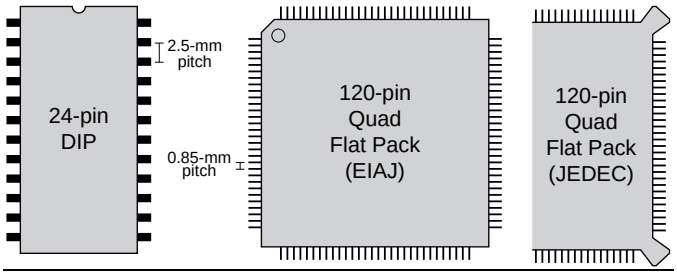

Figure 1. A quad flat pack can have many more pins than a DIP due to its smaller pin spacing. The JEDEC package differs from the EIAJ standard due to its corners. (Parts are approximately actual size.)

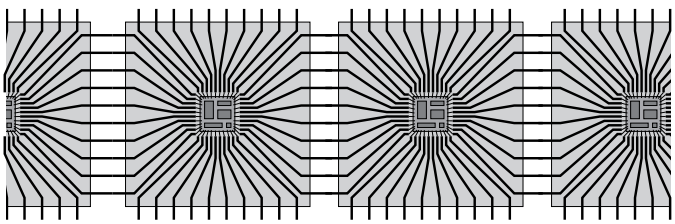

Figure 2. Top view of a set of lead frames with dice wire-bonded in place. These frames are ready to be covered with plastic to form the outer shell of the QFP part.

curl under the package to prevent damage. As shown in the figure, J-leads are wider than the PQFP's leads, limiting PLCCs to fewer than 100 pins. IDT's R3051, with only 80 pins, is available in a PLCC, as are many 8-bit and 16-bit microcontrollers.

Plastic packages have some disadvantages that are particularly critical for high-performance microprocessors. As these processors increase pin counts to 400, 500, even 600 pins, PQFPs cannot keep up. Plastic packages are also limited to 1–2 W of heat dissipation; the combination of high clock rates and high transistor counts puts most high end processors well beyond that limit.

A few 32-bit processors can accept the limitations of plastic packages. The most popular are 386 chips from AMD and other vendors. Intel, AMD, and others also sell 486 processors in PQFPs, although speeds above 33 MHz require a ceramic package for power reasons. The forthcoming R4200 MIPS processor also uses a PQFP.

Solving the Heat Problem

A simple plastic package is limited to about 1 W of power dissipation. This limit can be increased to about 2 W by embedding a heat spreader (sometimes called a heat slug) in the package above the die. The thermal conductivity of the metal spreader helps channel the heat from the die without damaging the plastic. This feature adds slightly to the cost of the package.

The plastic package has a high thermal resistance, which means that the plastic tends to keep the heat inside rather than dissipating it outward. One alternative is to replace the plastic exterior with a ceramic material, such as that used in a ceramic PGA. This material has a lower thermal resistance than plastic, reducing the cooling problem. For very hot chips, heat sinks can be attached easily to the ceramic surface.

While ceramic quad flat packs (CQFP) are occasionally used, they are much more expensive than plastic packages due to the cost of the ceramic. A CQFP is, however, less expensive than a CPGA because it requires fewer layers of ceramic. IBM's PowerPC 601, for example, uses a CQFP because its 9–12 W power dissipation rules out a plastic package, but its 304 signal pins just fit into the QFP form factor, saving cost compared to a PGA.

Another variant aimed at solving the heat problem is the metal quad flat pack (MQUAD). This device uses a metal shell that is attached to the lead frame by a nonconductive epoxy. The metal shell is similar in concept to a heat spreader but has a greater capacity for conducting heat away from the die. The shell can dissipate up to 6 W without a heat sink, or more with a heat sink. IDT offers MQUAD packages for its R3051 and R3081 processors; it provides a significant cost savings over the PGA version.

Although the metal itself is slightly more expensive than plastic to fabricate, the cost of MQUAD packages has been kept artificially high due to patent constraints.

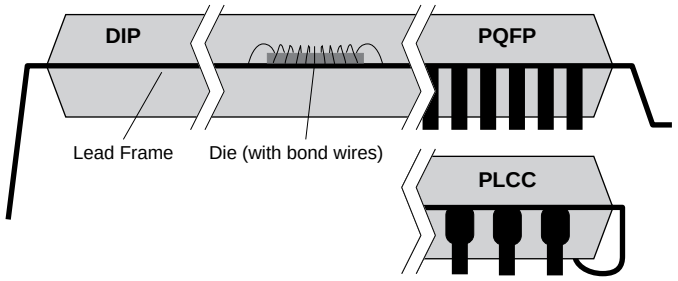

Figure 3. Side view of various plastic packages. Through-hole packages (left) use straight leads, while surface-mount packages (right) have flat leads that either spread out (PQFP) or tuck under the package (PLCC). The center section shows the die bonded to the lead frame and is common among all of these packages.

A company called Olin owns patent rights to the metal package and has licensed a limited number of vendors to produce these packages. Royalties and supply restrictions have kept the price of metal packages high, particularly for low-pin-count devices. MQUAD packages are still less expensive than ceramic, and approach the cost of plastic for the largest PQFPs. If the market situation changes, however, metal packages could become less expensive and much more popular.

Other QFP variations focus on reducing the package size. Intel's 3.3-V 486 chips are the most popular processors available in a "shrink" package (SQFP) intended for portable applications, particularly handheld devices. This package reduces the lead pitch to 0.5 mm from the 0.65 mm used in the PQFP i486. Placing the leads closer reduces the package size from 35 to 28 mm per side, a 36% reduction in area. The height of the package is also reduced, from 4.5 to 3.7 mm. The ARM610 uses a similar thin package (TQFP). These packages do not match any of the standard EIAJ or JEDEC sizes shown in Table 1; SQFP- and TQFP-type packages have vendor-specific dimensions.

As system vendors continue to cram more components into a smaller space, such variations on the standard PQFP will gain in popularity. One potential roadblock is the difficulty in reducing lead pitch below 0.5 mm. Smaller leads are more difficult to place accurately and to solder, and are more easily bent or damaged. PC

Lead Count	Body Size	Lead Pitch
100 pin	14 × 20 mm	.85 mm
120 pin	28 × 28 mm	.85 mm
144 pin	28 × 28 mm	.65 mm
160 pin	28 × 28 mm	.65 mm
184 pin	32 × 32 mm	.65 mm
208 pin	28 × 28 mm	.50 mm
240 pin	32 × 32 mm	.50 mm
304 pin	40 × 40 mm	.50 mm

Table 1. Specifications for common PQFP packages typically used for microprocessors. (Source: EIAJ)

Surface Mount Reduces Size

Historically, printed circuit (PC) boards have been built with through-hole technology (THT). This method handles discrete components (resistors, capacitors) and ICs in DIP packages. As indicated by the name, components are placed on the board by inserting their pins or leads through holes in the board, which then are filled with solder both to ensure a good electrical connection and to hold the part firmly in place. Because drilling small holes very close together is difficult, the pins on DIP parts are spaced at 0.1" (2.5 mm) intervals. As ICs became more complex, requiring more pins, the DIP design became impractical for chips with 80 or more pins. This led to the use of PGAs for these large devices. Since PGAs use pins with the same 0.1" pitch, they can be installed using the through-hole process.

A different manufacturing process, called surface-mount technology (SMT), was developed to reduce package size and thus board area. SMT attaches the leads directly to the surface of the board using a solder/paste mixture. Since no holes are needed, the leads can be closer together; typical pitches range from 1 mm to 0.5 mm or less. Taking advantage of this technology, DIP parts are available in small-outline packages variously called SOP, TSOP, VSOP, and other names, depending on the size and pitch. These packages reduce the physical size of a DIP part by up to 80%.

Surface mount increased the popularity of quad flat packages. With SMT's smaller lead pitches, QFPs achieved pin counts that previously required PGAs—and at a much lower cost. Most large devices now use PGAs only if it is not possible to use a QFP due to pin count or power dissipation.

Today, PC boards intended for space-critical applications (such as portable computers and consumer products) are almost entirely built using SMT components. Boards for larger systems typically use a combination of SMT and THT, but the trend is toward increased use of SMT. Looking at the unit volume of all ICs, ICE estimates that surface-mount parts will grow from 43% of the market in 1992 to 76% in 1997 and more than 80% by the end of the decade.

board manufacturers have experimented with 0.4-mm parts but there has been little acceptance of this type of package, particularly in the US. Many smaller manufacturers are still uncomfortable with even 0.5-mm leads.

PGAs Provide Power, Performance

Virtually all high-performance microprocessors use ceramic PGA packages, including the R4000 and R4400, SuperSPARC, the PA7100, the Alpha 21064 and 21066, and Pentium. These chips dissipate 10–30 W, preventing the use of low-cost plastic packages. The MIPS, HP, and Digital chips all require more than 400 pins for their wide, high-speed buses, another factor that eliminates the PQFP as an option.

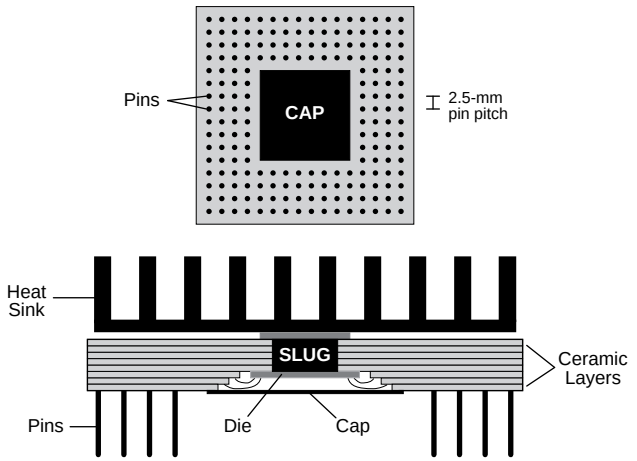

Figure 4. As shown at top, a pin-grid array (PGA) package has several rows of pins on the bottom. The cutaway view (below) shows the die mounted on layers of ceramic.

CPGAs are expensive to manufacture. Figure 4 shows that a CPGA consists of layers of ceramic material that contain traces used to route signals from the die to the pins. Each row of pins adds to the number of routing layers required; additional layers are used for power and ground. These power and ground planes also provide distributed bypass capacitance and help to isolate high-frequency signals, improving noise immunity. Overall, PGAs provide a better electrical environment than QFPs, allowing higher operating frequencies.

A CPGA's ceramic substrate must be built layer by layer. The substrate design is unique for each chip design, reducing economies of scale. As in a QFP, the die is placed in the center of the package and wire-bonded. A PGA usually has two or three tiers of bonding pads to accommodate the large number of signals. After bonding is complete, a metal or ceramic lid is affixed, hermetically sealing the die area. PGAs are sometimes called cavity packages because of the small open area around the die. Figure 4 shows a package with the cavity down, but some PGAs are built with the cavity on top.

Since CPGAs are designed for a single application, they are often further customized. Some HP processors, for example, have small bypass capacitors on the top of the package to improve high-frequency performance. Many chips use a heat slug, shown in Figure 4, to help conduct heat from the die to the heat sink. Of course, these modifications increase the cost of the package.

Although high-end microprocessors sell for hundreds of dollars, an expensive CPGA can still be a significant cost burden, but few high-end CPU designers are willing to accept the bandwidth limitations of a plastic package. A typical PQFP-based processor is limited to a 40-MHz, 64-bit data bus, or about 320 Mbytes/s of data bandwidth. In contrast, Digital's 21064 consumes over

1060 Mbytes/s of peak bandwidth, and the PA7100 requires 1600 Mbytes/s.

The upfront tooling for CPGAs is expensive, typically hundreds of thousands of dollars. The package design often takes several months and is done in parallel with the chip development; if the chip specifications (power, die area) change significantly during development, the package may need to be redesigned.

Ball-Grid Array Reduces Package Size

An alternative package that has recently garnered increased attention (but few design wins) is the ball-grid array. Instead of pins, a BGA uses an array of solder balls on the bottom of the package, as shown in Figure 5. This is similar to the old land grid array (LGA) package, which used small pads instead of solder balls. By using the entire underside for interconnect, BGAs can use less than half the area of an equivalent PQFP. It eliminates the need to move to a 0.5- or 0.4-mm lead pitch; the solder balls use 1.5-mm spacing, easing alignment problems. In fact, when the solder is heated, the package tends to align itself due to the surface tension of the solder-to-solder bonds.

Motorola developed this package, which it calls the overmolded pad array carrier (OMPAC), to reduce the size of ICs in portable communication devices. Plastic BGAs use a laminate base that is much like a single-layer PC board, to which the die is attached using standard wire bonding. The laminate has traces on the top and bottom sides that route the signals from the die to the balls, as shown in Figure 5. As in other packages, power and ground may use several leads each. A plastic or metal cap is attached to protect the die.

In addition to its compact size, the BGA has other advantages. The package height is reduced compared to a PQFP, making it suitable for applications such as Type I PCMCIA cards. The array of contacts simplifies the routing of signals on the board, compared to a fine-pitch QFP with contacts only around the edge of the part. The BGA's shorter leads potentially provide better electrical performance than a PQFP. Unlike a PQFP, a BGA has no pins, which are easy targets for bending.

The biggest potential drawback is that there have been no extensive, long-term tests to prove this new package's reliability. Thermal stress, moisture (like PQFPs, BGAs are non-hermetic), or unknown factors could cause problems down the road. According to BPA Technology, a research firm in Cold Spring Harbor, New York, about 16 million plastic BGAs were shipped last year. With this many parts entering the market, reliability data should be available within the next few years.

Other issues include the inability to inspect under-chip solder bonds and board manufacturers' lack of equipment to handle these devices. BGA devices are also quite difficult to debug, as the inputs and outputs cannot

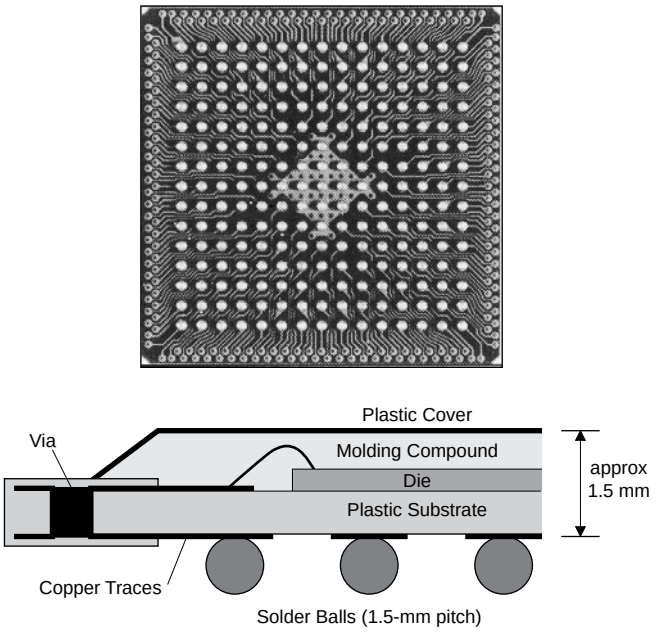

Figure 5. The photograph shows solder balls and traces on the bottom of a ball-grid array (BGA). The diagram shows how signals are routed from the die to the solder balls. (Source: Motorola)

be probed with a logic analyzer. One solution is an in-circuit emulator; Emulation Technology (Santa Clara, Calif.) has announced a set of adapters for BGA devices.

Motorola has patents on the BGA design, but the company plans to make them broadly available. Several major packaging vendors have licensed BGA technology from Motorola. Chip companies that are considering using BGAs expect that the package will be available from a number of vendors in the future.

Although BGAs seem well-suited for microprocessors that currently use PQFPs, Motorola has no immediate plans to market its standard processors in BGA packages. The company has distributed samples of its 68302, for example, in BGAs but received little interest. The company is producing a special version of its 68HC16 in a BGA for a single customer but has no plans to broadly market this version.

Intel also has no immediate plans to put 386 or 486 chips into BGAs. Other processor vendors are looking into this type of package but have no product plans yet. System vendors appear to be waiting to see how initial products work out before committing to a BGA processor.

IBM Moves POWER Processor to BGA

One vendor that is committed to the ball-grid array is IBM. Since 2Q93, the company has been building its RIOS-1 processor chip set (see MPR 8/21/91, p. 10) in BGA packages. The chip set, which is used in all of IBM's RS/6000 workstations, consists of six to eight chips (depending on the model), all of which have been moved to the new package. These chips have lead counts rang-

ing from 196 to 304.

The company has also shifted the processor and other components in some of its AS/400 minicomputers to the BGA package. These devices use packages with as many as 625 leads. Between these two programs, IBM expects to build 500,000 BGA devices in 1993.

Unlike Motorola, IBM is using ceramic BGA packages. These devices appear similar to the one in Figure 5 but use a ceramic substrate much like a CPGA. While the ceramic is more expensive than plastic, a CBGA is still much less costly than a CPGA due to its smaller size and lack of pins. A BGA can be up to 75% smaller than a PGA with the same pin count, which also reduces board area and board manufacturing cost. IBM uses a slightly reduced 50-mil (1.3-mm) pitch for its BGA packages.

IBM is using BGAs mainly to replace PGA packages, so the extra cost of ceramic over plastic is acceptable. The CBGA is hermetically sealed, avoiding any moisture problems that might occur with the PBGA. The ceramic package is also easier to cool; the RIOS-1 chips, using small heat sinks, dissipate up to 6 W each.

The company says that extensive prototyping detected no reliability problems with the new packaging, and that its board assembly lines require no new equipment to place, test, and inspect BGAs. Other PC board vendors, however, may not be as well equipped as IBM.

Looking to the future, IBM says that it will market some versions of its PowerPC processors in CBGA packages. The company would not specify which versions, but said that the package is best suited to high-performance chips and that it will be deployed by 1994. This description fits the PowerPC 604 and possibly the 620. Motorola would not commit to matching IBM's BGA offerings, saying only that such a move is a "possibility for the future."

Conclusion

Packaging is an important aspect of microprocessor design. These chips are running at increasingly high frequencies, and the package must be designed to dissipate the heat generated at such speeds. When data is communicated outside of the chip, the electrical characteristics of the package help determine how fast this transfer can proceed.

The emphasis on ever-smaller portable systems is driving chip vendors to reduce the size of their devices. While PQFPs offer a smaller footprint than PGAs, the new PBGA is even smaller and may come to replace the PQFP in portable applications. Other alternative packages (that will be discussed next issue) are yet more diminutive, leaving the future of the PBGA in doubt.

IBM's aggressive move into CBGAs indicates that these packages may come to replace PGAs due to lower cost and smaller footprint. Other vendors may wait to see how the new package performs before jumping aboard the bandwagon. ♦

*Next issue, we will discuss other alternatives to standard packaging, including tape automated bonding, chip on board, and multi-chip modules (see **071304.PDF**).*

