AT&T Expands Hobbit Family

Higher Performance, Higher Integration Versions Now Sampling

by Linley Gwennap

After announcing its first Hobbit processor a year ago, AT&T announced three new family members at the Microprocessor Forum. These new chips will expand the breadth of Hobbit-based system options, allowing for smaller, less expensive devices as well as more powerful versions of existing products, such as Eo's Personal Communicator *(see **061509.PDF**)*.

Rob Franzo, presenting for AT&T Microelectronics Group at the conference, pointed out that the new processors include twice as much on-chip memory, which boosts performance by about 20%. To reduce cost and physical size, AT&T now offers two- and three-chip configurations to go with the original four-chip design. These chip sets include all the system logic and peripheral interfaces needed for a typical PDA.

92020S Improves Performance

Figure 1 shows the new family of Hobbit products. The original chip set was dubbed the 9201x and consisted of the Hobbit CPU plus three system-logic chips and an optional ISA interface chip. The second-generation parts are denoted in the figure as the 9202x series.

The highest-performance option is the 92020S processor chip, which is binary- and pin-compatible with the original 92010 CPU. The most significant enhancement is that the size of the on-chip instruction cache (which AT&T calls the prefetch buffer) has been expanded from 3K to 6K.

The larger cache provides a moderate performance increase. AT&T rates the 92020S at 16 Dhrystone MIPS at 20MHz, compared to 13.5 for the 92010. PenPoint applications, currently the primary software base for Hobbit, could see an even greater boost; this object-oriented software has shown poor hit rates in the 92010's 3K cache.

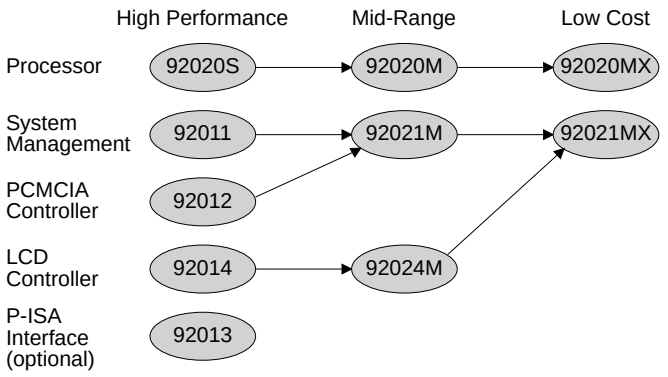

Figure 1. The new Hobbit family includes a high-performance option (92020S) and two high-integration options, the 92020M and 92020MX chip sets.

By reducing the number of accesses to off-chip memory, the expanded cache also decreases CPU power usage. The new processor is rated at 210 mW, about 20% less than the 92010. With fewer memory accesses, power is reduced in the memory subsystem as well.

The 92020S includes a second enhancement, the Wait For Interrupt instruction. This instruction can be used by power-management software to put the CPU into a low-power state in which no instructions are executed. Any external interrupt causes the CPU to quickly resume instruction execution.

Since the 92020S is pin-compatible with the 92010, it uses the same system-logic chips as its predecessor, including the 92011 system-management controller, the 92012 PCMCIA controller, and the 92014 video-display controller. The 92013 provides an optional bridge to ISA peripheral chips.

Multiplexed Bus Reduces Pin Count

The new mid-range solution is called the 92020M. The "M" stands for multiplexed, indicating that this chip set uses a new multiplexed bus in place of the original Hobbit system bus. The 92020S supports a 32-bit address bus and a 32-bit data bus; the 92020M combines these into a single bus, eliminating 30 pins from each device in the chip set.

The multiplexed bus has the disadvantage of being slower; each transaction requires an extra cycle to transmit the address and data separately, although a new burst mode helps somewhat. AT&T rates the 92020M at 13.5 MIPS, about 20% slower than the non-multiplexed 92020S and the same speed as the original Hobbit.

The new bus uses active-high signals rather than the active-low protocol of the original Hobbit bus. Rob Franzo said that since the bus signals are at a low voltage when inactive, it's easier for external power management to turn off the system during inactive periods.

The lower pin-count of the multiplexed bus allowed AT&T to combine the PCMCIA and system-management functions into a single chip, the 92021M. The number of PCMCIA slots is reduced from four to two with this chip set. A separate graphics chip, the 92024M, is used in this configuration; it is essentially identical to the 92014 except for the multiplexed bus.

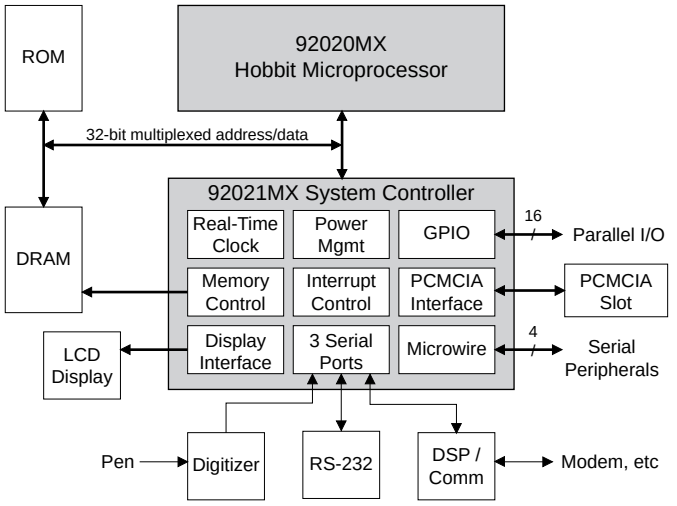

Figure 2. The smallest Hobbit system requires just two main chips using the 92020MX chip set.

The M-family chips include a few other enhancements. The new bus includes dynamic sizing for 16-bit as well as 32-bit-wide memories. The number of general-purpose I/O pins is increased from 8 to 16 on the system-management chip. A new serial port, using the standard Microwire protocol, can be connected to an external power-management controller. Note that there is no 92013M; ISA peripheral chips are not supported by the M-family chip set.

Two-Chip Set for Minimum System

Figure 2 shows the third new Hobbit chip set, the MX, which uses only two chips to implement a minimum system. The 92020MX processor is identical to the 92020M except that the instruction cache is only 3K, the same size as the original Hobbit processor. The smaller cache, combined with the multiplexed bus, reduces performance to 11.5 MIPS. Power consumption increases to 290 mW due to the added bus accesses from the smaller cache and extra state changes on the multiplexed bus.

The 92021MX crams the display controller onto the system-management chip. To keep the pin count within a 208-pin PQFP, the MX chip set sacrifices one PCMCIA slot and support for a VRAM frame buffer and 1024×768 ×8 CRT displays (both of which are included in the 92014 and 92024M). The MX maintains the graphics frame buffer in DRAM as part of the system memory, forcing the system bus bandwidth to be shared between graphics and program accesses. The MX supports LCD displays up to $640 \times 480 \times 16$.

Figure 2 shows that a minimum Hobbit system includes one PCMCIA slot, an LCD display with pen input, a standard serial port, and a communications interface. This interface can connect to a modem complex—including a DSP and codec—for analog data transfers over a phone line. With a radio front-end, the system could also support wireless communications for voice or data.

New Process and Packaging Reduce Size

All the new chips are built in what AT&T calls a 0.6-micron, two-layer-metal CMOS process. This process uses the same metal geometries as the 0.9-micron process employed for the original Hobbit chips, and so offers no die size improvement. In fact, with the larger cache and support for the new wait instruction, the 92020S/M die is 125 mm^2, 36% larger than the original 92010S. Even the 92020MX is 103 mm^2, still larger than the 92010S. The 92020 processors are all available in either a 132-pin PQFP or a 144-pin TQFP that reduces the package area by 30%.

Franzo says that the process change was made to improve transistor speed, yet the new parts run at the same frequency as the original Hobbit chips. This implies that future, faster chips using the 0.6-micron process may be announced. AT&T plans to move the chips to a "true half-micron process" next year, greatly reducing die size and manufacturing cost while further increasing performance.

Table 1 summarizes the characteristics of the three new chip sets. The Hobbit family now spans a performance range of 11.5 to 16 MIPS and a price range of $63 to $101. The low-cost chip set requires just two chips but sacrifices CRT graphics support and all but one PCMCIA slot. Although the table shows the 3.3-V specifications, the new chips also run at 5 V, boosting the clock rate to 30 MHz.

	92020S	92020M	92020MX	Polar	Am386SC
Clock Rate	20 MHz	20 MHz	20 MHz	33 MHz	33 MHz
Dhrystone MIPS	16 MIPS	13.5 MIPS	11.5 MIPS	6 MIPS	6 MIPS
On-Chip Cache	6K	6K	3K	2K	none
Memory Bus	32 A, 32 D	32 mux'd	32 mux'd	22 A, 16 D	22 A, 16 D
Voltage	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
CPU Power*	210 mW	250 mW	290 mW	550 mW	550 mW
Number of Chips	4 chips	3 chips	2 chips	3 chips	1 chip
PCMCIA Slots	4 slots	2 slots	1 slot	1 slot	2 slots
Serial Ports	3 ports	3 ports	3 ports	2 ports	1 port
Parallel Ports	none	none	none	none	1 port
LCD Support	640 x 480	640 x 480	640 x 480	640 x 480	640 x 400
CRT Support	1024 x 768	1024 x 768	none	none	none
Frame Buffer	separate	separate	shared	shared	separate
Chip Set Power*	530 mW	490 mW	390 mW	600 mW	550 mW
Chip Set Price	$101	$80	$63	$58	$49
Availability	1Q94	1Q94	1Q94	1Q94	2Q94

Table 1. The three new Hobbit chip sets differ primarily in performance, price, number of PCMCIA slots, and graphics support. VLSI's Polar chip set and AMD's 386SC offer significantly lower performance due to their 386 processor cores. As shown here, the Polar chip set includes one external PCMCIA chip to even the comparison. (*Power numbers are typical ratings with a 50-pf bus load.)

Hobbit Outperforms Polar, 386SC

Table 1 also compares the new Hobbit chips with the recently announced Polar chip set from Intel and VLSI *(see **071302.PDF**)* and AMD's 386SC *(see **071404.PDF**)*. While Polar is clearly designed for PDAs, the 386SC is intended more for handheld PCs running DOS or Windows. The two markets are quite similar, however, and AMD has the ability to quickly redesign its chip for pen-based PDAs.

The most striking difference between the Hobbit chip sets and the others is performance; even the slowest Hobbit is nearly twice the speed of Polar or the 386SC on the Dhrystone benchmark. This advantage is due to the newer RISC-like design of the Hobbit processor *(see **060201.PDF**)*; the other two chips use older 386SX processor cores that are hampered by x86 compatibility.

While the Dhrystone benchmark is not always a good measure of actual performance, the Hobbit processors have more on-chip cache than the x86 chips, which should improve performance on real applications. Like the x86 processors, Hobbit uses variable-length instructions to increase code density; AT&T claims that Hobbit binaries are about the same size as equivalent 386 binaries. The two x86 chips will be hampered by their 16-bit interfaces to memory.

The Hobbit MX chip set is roughly equivalent to the others in the number and type of supported peripherals. It costs about the same as the x86 products and uses a third less power. Thus, the MX delivers a two-to-one advantage in overall performance, performance per watt, and price/performance.

Rob Franzo of AT&T Microelectronics describes the three new members of the Hobbit processor family.

Although AT&T's 92020S and 92020M chip sets are more expensive and require more board space than Polar or the 386SC, they also offer better graphics and more PCMCIA slots. All the Hobbit chip sets include a third serial port, making it easier to add built-in communications. The "S" and "M" processors also widen the performance gap over the 386-based chips.

Other PDA Processors Still Unclear

Other PDA processors have been announced, including ARM's 610, Motorola's 68349, Hitachi's SH7032, and NEC's V820. It's difficult to compare the new Hobbit chips to these products, however, because of a lack of information on their support chips.

Inside a Newton, the ARM610, combined with Apple's "Runt" ASIC *(see **071303.PDF**)*, forms a two-chip set with features comparable to the Hobbit chips. Since Apple has not released power or pricing information for its ASIC, it is impossible to compare these important aspects of the ARM solution. We do know that the performance of the ARM610 is slower than Hobbit's performance at the same voltage.

The 68349 *(see **070803.PDF**)* alone does not provide a complete set of PDA features; it will be combined with General Magic's Astro chip, about which little is known. The processor includes a large 6K cache on-chip and a 32-bit memory interface, but performance is restrained by the outdated CISC core, which delivers about 6 MIPS at 16 MHz and 3.3 V.

Like the 68349, NEC's new V820 *(see **071405.PDF**)* has no PCMCIA or graphics support, requiring an ASIC to complete the system. As announced, the part operates only at 5 V, using 750 mW of power, far more than the 3.3-V Hobbit chips. NEC is working on a 3.3-V version that could have performance and power ratings comparable to the 92020MX. At a list price of $80, the NEC chip is far more expensive than the MX, even without considering the cost of additional peripherals.

Hitachi's SH7032 *(see **070802.PDF**)* is limited to just 12.5 MHz at 3.3 V, at which it delivers 10 MIPS. Although it includes a large 8K on-chip RAM, the chip uses a narrow 16-bit interface to external memory. It is aggressively priced at $33 but requires an external ASIC for graphics and PCMCIA.

The new Hobbit chips deliver the highest performance of any 3.3-V PDA processor. Only AT&T, AMD, and the Intel/VLSI team offer openly available chip sets with a full set of PDA interfaces, and the AT&T chips easily outperform their 386-based rivals. While other vendors are just entering the PDA processor market, AT&T now offers a range of chip sets with varying performance and integration options. Future 486-based chip sets could present a stronger challenge to Hobbit, but for now the new chips have established leadership positions among PDA processors. ♦

Price and Availability

Pricing for the new Hobbit chip sets appears in Table 1. The ISA chip (92013), not included in the 92020S chip set, is priced at $25. The 92020S Hobbit CPU is available for $37; the 92020M for $34.50, and the 92020MX for $32. All pricing is for volumes of 10,000.

Contact AT&T Microelectronics at 4995 Patrick Henry Drive, Santa Clara, CA 95054; 408-980-3700, fax 408-980-3796.

