SHARC: A Bold New DSP Thrust by Analog

Analog Devices' Floating-Point Chip Sets New Integration Level

by Linley Gwennap

Analog Devices announced at this year's Microprocessor Forum a new, highly integrated DSP chip. The ADSP-21060 is the first of the SHARC (Super Harvard Architecture Computer) family, an extension of Analog's existing ADSP-21000 family of 32-bit floating-point processors. Its most notable features are a massive 4-Mbit on-chip static RAM and an I/O processor with 10 DMA channels. The 21060 is Analog's first high-performance, multiprocessing device.

Most DSP chips have modest on-chip RAMs of up to 128 Kbits. With its much larger memory, the 21060 could be called a microcontroller instead of a microprocessor. While at first glance this new integration is similar to the development of the general-purpose microcontroller, the 21060 is not assured of the same success. Analog was able to make this major departure by securing funding from MIT Lincoln Laboratories, which plans to use it in a multiprocessor radar system.

Due to MIT's influence, the 21060 is suited for very high-performance multiprocessor applications, but Analog also included many general-purpose features. The company plans to develop future versions with smaller on-chip memories for lower-cost applications. First, it must complete the design of the 21060, which has not yet been fabricated. Given this status, the performance figures for the chip are only preliminary estimates.

Multiple Functional Units

The core processor of the 21060 is the third refinement of the 21000 family, following the '010 to '020 half-generation step. It remains instruction-set compatible with minor but important enhancements. As the most recent DSP architecture among the major suppliers—including TI, Motorola, and AT&T—the 21000 uses higher transistor counts to include more functions, which in turn increase performance significantly.

For example, as shown in Figure 1, the 21060 uses a large 10-port register file to feed three computation elements at the same time. The 32-bit and 40-bit extended-precision floating-point arithmetic is true IEEE format, not simply converted during I/O. The dual address generators support complex addressing modes like bit-reverse for FFTs and modulo addressing for circular buffers. These modes are all supported for multiple channels and have flexible sizes and boundaries.

Performance is enhanced by single-cycle instruction execution and zero-overhead looping. The single-cycle instructions also simplify programming the 21060. The 32-word instruction cache reduces bus accesses during the tight inner loops common in DSP algorithms, leaving the core's shared dual-bus structure for data accesses. Instructions are 48 bits each, enabling direct control of all arithmetic and address-generation units on each cycle. This orthogonal instruction set simplifies the compilers for high-level languages.

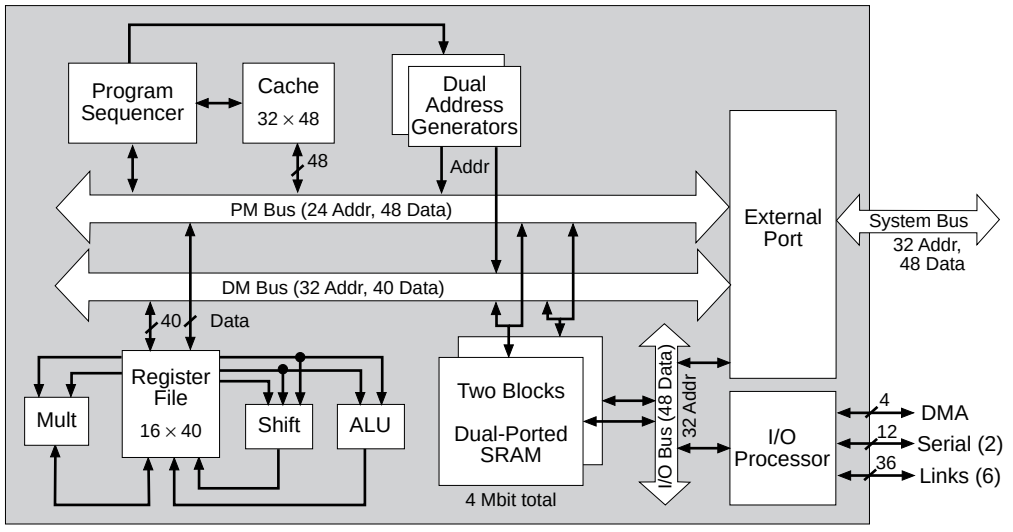

Figure 1. The ADSP-21060 features dual internal buses and a dual-ported 4-Mbit static RAM that takes most of the die area.

The 21060 is designed for a 0.6-micron, two-layer-metal CMOS process, which is expected to provide an instruction cycle time of 25 ns, delivering 40 MIPS. A sustained rate of 80 MFLOPS is possible, with a peak of 120 MFLOPS on register data. The major advantage of the advanced IC technology, however, is that it can integrate 4 Mbits of dual-ported static memory on the 275 mm^2 (22 × 12.5 mm) die. The transistor count exceeds 25 million and power consumption is estimated to be 3.6 W. The initial production foundry is Sharp Microelectronics.

Large SRAM with Processors Attached

The huge on-chip memory is organized into two 2-Mbit blocks, each of which is dual-ported and independently configurable into groups of 16-, 32-, or 48-bit words. The 48-bit mode is for program or extended-precision data, and the 16-bit mode is for a new short-word format. As shown in Figure 1, one port of each block connects to the processor, and the other connects to the external I/O port. A 32-bit (4G-word) address space covers the external memory as well as, in multiprocessor configurations, the internal memory of other processors.

A standard Harvard design would reserve one block for data and the other for instructions. The SHARC design, however, allows the full memory to be used as desired. The small instruction cache reduces collisions between instruction and data accesses. The single bus to external memory is unlikely to be a bottleneck due to the large amount of on-chip storage.

This careful matching of processor capabilities and memory allows the 21060 to perform a complex 1024-point fast Fourier transform (FFT) in a record time of 0.46 milliseconds. The benchmark uses a radix-4 algorithm that takes up only a small portion of the available memory for data; most other processors running this algorithm have little on-chip memory left for buffering and other processing.

The I/O processor's 10 DMA controllers operate independently of any programmed transfers using the I/O port of the two memory blocks. DMA can be used with any of the three types of I/O ports: the two bidirectional serial ports, the six 4-bit-wide link ports, or the 48-bit-wide external port. The external port provides a system bus to external memory, a host CPU, or other 21060s in a multiprocessor configuration. All the ports are fast: the serial ports operate at 40 Mbits/s; by performing two transfers per cycle, the link ports each deliver 40 Mbytes/s.

The link ports allow direct interprocessor communication in multiprocessor configurations, as shown in Figure 2. Up to six processors, plus a host, can be attached in a cluster configuration (with each 21060 connected to all others). Larger numbers of processors can be organized in three-dimensional arrays, in which each 21060 can directly communicate with its six nearest neighbors. No glue logic is required in either type of configuration.

The 21060 includes many features for multiprocessing in addition to the link ports and shared memory. The chip provides bus arbitration logic with selectable priority schemes, bus-lock sequences for implementing semaphores, and a broadcast mode to all processors.

Cost-Effective Applications

With the dramatic growth in digital signal processing, there are many potential applications for this new combination of a fast floating-point processor with a large on-chip memory. Floating-point processing is generally used where the dynamic range is large. There are also applications with moderate dynamic range but where the large size of the data set and the amount of processing requires floating-point to maintain adequate precision. Graphics and image processing are prime examples of applications with large bodies of data requiring extensive processing but with limited output dynamic range.

Applications for the 21060 can be divided into two categories: single-chip and multiprocessor configurations. For single-chip designs, the central issue is whether 4 Mbits is enough data memory for the benefits of speed and integration to pay for themselves. The 21060's large memory (configured, for example, as 16 Kwords of instructions and 96 Kwords of 32-bit data) is enough for many speech and telecommunication applications. For image and video processing, however, this configuration allows a resolution of only 300 × 300 pixels, low even by consumer-device standards. A single 21060

Price and Availability

Sampling of the ADSP-21060 is planned for May of 1994 with a target price of $296 for the 40-MHz version in 1000-piece quantities. It will also be available with a 33-MHz clock rate. Packaging is in a 240-lead PQFP. A 3.3-V version is expected to be announced in the second half of 1994.

The ADSP-21060 simulator is available today for $695 or with the C and Numeric C compilers, assembler, linker, debugger, libraries, etc., for $995. The in-circuit emulator and evaluation board are expected in the second quarter of 1994.

For more information, contact Analog Devices (Norwood, Mass.) at 617.461.3881; fax 617.821.4273.

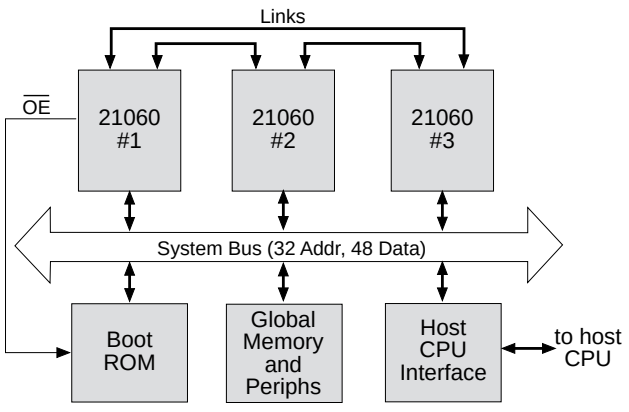

Figure 2. Several 21060 chips can be connected using the serial link ports in a cluster or three-dimensional array. System memory and peripherals are supported without any external glue logic.

may be performance overkill for most voice applications (except for the very high end) yet it has too little memory for most other high-volume multimedia applications.

As a multiprocessor element, the 21060's fast processing speed, high I/O bandwidth, and large local memory are a natural fit for graphics and imaging applications, which are high-volume and cost-sensitive. The memory size suits the more common coarse-grain parallel processing of today's compression algorithms, and there should be few I/O bottlenecks. A single 21060 performs an 8 × 8-point discrete-cosine transform (DCT) in only 6 µs.

The highly integrated 21060 will allow large numbers of processors to fit into a desktop workstation. An advantage of the multiprocessor design is that users can start with a small number of chips and add more as their need for performance increases.

Why Not a RISC Instead?

When examining a special-purpose chip such as the 21060, it is natural to question whether signal processing can be done just as well (and less expensively) with a high-volume RISC processor. This requires careful analysis, but the 21060 has some unique advantages compared to most RISC chips.

MICHAEL MUSTACCHI

Analog Devices' Kevin Leary describes his company's partnership with MIT Lincoln Labs.

The 21060's small instruction cache is tuned for the tight inner loops found in many DSP algorithms. In contrast, the large instruction-only caches in most RISC processors are wasted for these algorithms. The 21060 also provides superior real-time performance due to fast context switching and interrupt servicing. The bit reversal and modulo address modes in the Analog chip are useful for many DSP applications and are not found in most RISC processors. Finally, the fast I/O, multiported memories, and parallel data paths also enhance DSP performance in the 21060.

It is difficult to compare the number of operations per second, but the 21060 can perform several operations in a single cycle—such as complex address calculations, bit shifting, and FP multiplication—that require multiple cycles on most RISC processors. Also, the higher level of integration can result in size, cost, and performance advantages for many applications.

For multiprocessor systems, the 21060 can be used to build large arrays of processors with no glue logic. Among RISC chips, only Inmos' Transputer implements an equivalent to the 21060's link ports. Thus, the Analog device can be used in multiprocessor configurations more easily than a standard RISC processor.

Analog's Competitive Advantage

TI dominates the floating-point DSP processor market as well as the fixed-point market. Its TMS 320C3x line requires external memory but is aggressively priced to compete at the system level, except where small size is critical. TI's 'C4x line has dedicated interprocessor communication and is the established standard for multiprocessors, providing the only real competition for the 21060. Both TI product lines have small on-chip memories relative to the 21060, with total program and data memories of under 100 Kbits.

At 50 MFLOPS, the latest version of the 'C31 has significantly lower performance than the 21060. But the TI chip, at less than $80 in thousands, has attractive price/performance compared to Analog's price tag of $296, even considering the cost of external memory for the 'C31. The 21060 has significantly higher raw performance than the 'C4x, and this advantage should be even higher for applications that take advantage of the 21060's larger on-chip memory. With its superior multiprocessor features, the Analog part has a clear advantage over the 'C4x, particularly since performance is more important than cost in many high-end, multiprocessor applications.

AT&T's DSP3210 is low-cost processor that targets PC multimedia applications and is priced aggressively. Multiprocessor operation is through shared memory only, without any interprocessor communications paths, although the AT&T chip had earlier success in multiprocessor graphics applications. At 33 MFLOPS, the '3210 delivers less than half the performance of the 21060, but it is less expensive even with external memory. AT&T has also added peripherals and interfaces to adapt the part for the PC market.

Motorola is now in the second generation of its DSP96000 floating-point family. Like AT&T's chip, Motorola's design has only shared-memory multiprocessor capability and a small on-chip memory. At 40 MFLOPS, it is slightly faster than the AT&T chip but still far behind the 21060.

Of the RISC offerings, only Intel's 860 has a significant installed base in floating-point DSP applications and that only in large multiprocessor systems, such as military applications. Like most RISC chips, the Intel processor was not designed for real-time applications; the 860 also suffers from Intel's recent lack of emphasis on this product line. With Analog's lower cost and support of Numeric C, the company may be successful against the 860 in these big systems.

Taking Performance to a New Level

With the 21060, Analog sets a new level of floating-point performance. The company becomes a late but well-equipped player on the multiprocessor field and puts a complete DSP system on a chip at a useful, but untried, price/performance point. It is most likely to succeed in multiprocessor applications for graphics and imaging, such as that envisioned by its backer, Lincoln Labs.

The 21060's large on-chip RAM and extensive I/O structure delivers high performance and allows a variety of systems to be easily configured. This ease of use, along with high-level-language tools, can provide fast time-to-market and early success for new system developers. Analog already reports design wins in cellular-telephone base stations and as a floating-point accelerator.

Future versions, which will probably be funded entirely by Analog, will naturally be aimed at less speculative, better-understood applications. In particular, the cost must be reduced for the part to reach volume portions of the DSP market. Analog says that the next version will have no more than 512 Kbits of memory (in the same organization) and this will reduce the cost of the chip, broadening the range of applications.

The company now has a set of functional blocks that can be quickly configured for a variety of floating-point applications. For example, true single-chip systems would benefit from on-chip ROM and more serial ports. Lower-cost versions could get by with a smaller external address space, fewer link ports, and no multiprocessor support.

Each successive application wave in DSP has had its effect on processor configurations, first with modems and currently with cellular telephones. Multimedia, including wireless communication, is clearly the next wave. While the initial member of the SHARC family is aimed at high-performance applications, future versions could be well-suited for the emerging multimedia market. ♦

Thanks to Bob Owen for researching and helping to put together this story.

