Most Significant Bits

HP Describes Plan to Regain Performance Lead
After watching Alpha, MIPS, and POWER processors surpass the performance of its best PA-RISC chips, HP has finally unveiled a strategy to boost its own performance. The company has announced the PA-7150, which it plans to ship in 2Q94 and rates at more than 135 SPECint92 and 200 SPECfp92. The new chip runs at 125 MHz and is functionally equivalent to the current PA-7100 CPU, which is limited to 99 MHz. As in the past, HP has no plans to market the 7150 as a chip but will deploy the new CPU in its workstation products.

To increase the clock rate, the design team did extensive testing at voltage and temperature extremes to locate critical speed paths throughout the 7100 design. Improving these speed paths required a full turn of the mask set, although most of the circuitry is the same. The 7150 uses the same 0.8-micron CMOS process as its predecessor, but minor process improvements over time have helped improve the frequency yield. Since the 71x0 relies on external SRAM for its single-cycle primary cache, 125-MHz systems require 7-ns memory chips, with a single 6-ns part used for one critical column.

In addition to the fast clock, compiler enhancements play a large role in the 7150's performance. If the new part achieves its goals, it will outperform Digital's 200-MHz 21064 on both integer and floating-point SPEC ratings, making the 7150 the fastest chip for integer work and the second-best (behind IBM's Power2) for floating-point. Digital expects its 225-MHz 21064A to reach production in July, however, so HP's lead may be short-lived. Still, the new announcement shows that HP is serious about the high-performance market and intends to remain competitive.

To further emphasize this point, the company revealed a roadmap of its future processor efforts. The next new design, dubbed the PA-7200, will include two integer ALUs and bi-endian support. According to an ISSCC abstract, the 7200 will reach speeds of 140 MHz. Performance is said to meet or exceed that of Digital's 275-MHz 21064A, which is expected to hit 170 SPECint92 and nearly 300 SPECfp92. The 7200 has already taped out and should begin shipping in systems by 4Q94.

After that, HP's roadmap gets somewhat fuzzy, showing performance increasing over time with product names like PA-8xxx and PA-9xxx. The latter is said to implement a "post-RISC" architecture combining aspects of superscalar processing with the VLIW technology described by HP's Josh Fisher at the recent Microprocessor Forum *(see **071604.PDF**)*. Since this architecture will require a new instruction set, compatibility will be retained through binary translators. The 9xxx chips may not be seen until 1997 or 1998.

HP will also continue to build chips for low-cost systems, starting with its 7100LC *(see **061504.PDF**)*. The company says that the 7100LC will begin shipping in systems in 1Q94 at clock rates of 60 and 80 MHz. At the faster speed, the 7100LC is said to deliver 84 SPECint92 and 130 SPECfp92, outrunning other low-cost chips. The new workstations are expected to start at less than $5,000 when fully configured. (Our next issue will contain additional information on the 7100LC, including a description of its multimedia enhancements.)

Cyrix Deploys 386SX Upgrade Chip
Following its end-user upgrades for 386DX systems, Cyrix is now selling a device to upgrade 386SX boxes as well. The original 386DX upgrade, dubbed the 486DRx^2 *(see **0710MSB.PDF**)*, contains Cyrix's 486DLC processor and a clock doubler. It plugs into the CPU socket in a 386DX system, offering approximately twice the performance. But since 386SX processors are typically soldered on the motherboard, it first seemed that users with these systems were out of luck.

Cyrix's new 486SRx^2 uses an innovative device, co-developed with Augat, that clips onto the 386SX, giving the upgrade chip access to all motherboard signals. The new upgrade takes advantage of the FLOAT pin on the 386SX to disable the existing processor. The upgrade works with all 20-MHz and 25-MHz 386SX chips, as well as with 16-MHz chips built since 1991. (Earlier versions do not have the FLOAT pin.)

Both the 486DRx^2 and 486SRx^2 are available to end users through retailer CompUSA as well as several major distributors and customer-service providers. The 25-MHz 486SRx^2 has a suggested retail price of $299, while the 20-MHz 486SRx^2 lists for $269.

NEC Puts R4400 in Multichip Module
Becoming the first merchant vendor of a RISC multichip module (MCM), NEC has announced the MR4401, which combines a 150-MHz R4400SC processor with 1M of secondary cache in a single package. By combining the cache on the module, the device fits into the 179-pin PGA package used by the R4400PC, allowing it to be plugged into existing designs. The design reduces the footprint of the MIPS processor while delivering the speed of a large secondary cache.

Many observers have predicted that processors will move toward MCM technology as CPU-to-cache speeds increase. A few years ago, Intel marketed an MCM containing a 486DX-50 with cache to help system vendors used to working with 25- or 33-MHz buses, but the product was too expensive for PCs; the DX2 processors proved to be a much more popular solution. NEC's module uses

a 75-MHz bus to its external cache, an even more severe challenge for systems using discrete parts. As with the Intel module, NEC's price could be a drawback; the company has not set a volume price for the MR4401, but samples cost a steep $3,000. Unless NEC can bring the price down significantly, its module will be too expensive for MIPS-based PCs, and workstation designers, who are familiar with fast caches, will probably choose to buy discrete SRAMs and save the money.

Other RISC vendors have had limited success with MCM packaging. Ross Technology manufactured a custom processor module, designed by nChip, for Tadpole's SPARC notebook *(see **071304.PDF**)*; for this product, the goal was to reduce the footprint of the processor, and Tadpole was willing to pay a bit more. IBM is packaging its multichip Power2 processor *(see **071301.PDF**)* into a ceramic module, but this design is intended for low-volume, high-priced servers. Neither of these RISC modules has been offered on the open market.

NEC, IBM, and Ross (then a subsidiary of Cypress) share a common advantage: an in-house supply of SRAM chips. In fact, all the dice in their modules are internally sourced. This simplifies the manufacturing and testing considerations but still may not reduce the cost enough to make the product appealing to a wide audience.

Taiwanese Vendors Back PowerPC

A group of Asian computer suppliers has formed the Taiwan New PC Consortium (TNPC) to support the PowerPC architecture. The members include system vendors Tatung, Mitac, and DTK; peripheral-card vendors Umax and FIC; and UMC, an IC vendor. None of the companies revealed specific product plans, but it appears that the system vendors will build PowerPC-based systems, probably using the recent Prep specification *(see **071704.PDF**)*, and UMC may develop system-logic chip sets or other interface chips.

Conspicuous by its absence is Acer, the largest PC vendor in Taiwan, which has already signed up for the MIPS platform. According to Motorola, Taiwanese companies build 70% of the motherboards for the worldwide PC industry; since these boards are then sold in systems by other vendors, however, the companies in TNPC will add little to the marketing presence of PowerPC. The consortium does give Motorola and IBM a voice in the hot Asia market and, if the demand for PowerPC systems increases, a high-volume, low-cost supply of system-logic chips and motherboards.

Cirrus Gains ARM License

As expected *(see **0705MSB.PDF**)*, Cirrus Logic has acquired a license to use core processors from Advanced RISC Machines (ARM) in future products. Cirrus had previously announced that it is developing system-logic chip sets for future Newton products; the new license allows the company to eventually combine the CPU core and system logic onto a single chip for very compact, low-cost Newton devices.

The first chip set from Cirrus will be two or three chips and will not include the ARM core; this chip set will be used in second-generation Newtons. The single-chip product probably will not be available until 1995. The latest agreement shows that Cirrus (and ARM) expect to be long-term players in the Newton market. The availability of system-logic chip sets from Cirrus will encourage third-party developers of Newton hardware.

Cirrus joins VLSI Technology, GEC Plessey, Sharp, and Texas Instruments as ARM licensees. Although this lineup seems too large for a somewhat obscure architecture, the companies are aiming for high-volume, but slightly different, markets. Plessey, soon to be joined by Sharp, is supplying chips for consumer products, including high-profile wins in the Newton and the 3DO game system. VLSI is aiming for embedded applications, and TI is focused on very inexpensive chips, primarily for the automotive market. With Cirrus to specialize in Newton chips, there may be enough room for all five vendors.

PCI License Issue Resolved

Apparently ending fears that Intel would use its patent portfolio to limit use of PCI with processors made by its competitors, the PCI Special Interest Group has released the long-awaited license agreement to accompany the 2.0 revision of the bus specification.

The wording of the agreement has been hotly debated in the PCI steering committee. The agreement was supposed to be released along with the specification early last spring, but it didn't materialize. Other self-imposed deadlines came and went, but at Comdex in November, the agreement finally emerged. The delays apparently were due to conflicts between PCI advocates pushing for a broad license and Intel's lawyers, who sought to limit the amount of Intel's intellectual property granted to PCI members.

A one-page agreement accompanied the original PCI version 1.0 specification, but this agreement did more to raise fears than to reassure. The key concern was that it granted rights only under three specific pending Intel patents and gave no assurance that Intel did not have other patents or patents pending that could limit use of the bus. Given Intel's reputation for using its intellectual property as a weapon against competitors, companies such as Digital and AMD were understandably concerned.

The new agreement, now six pages long, does not refer to specific patents at all, but rather to all patents that "relate to bus technology and are necessarily required to implement any implementation compliant with the PCI Local Bus Specification or Future Revisions." Rather than being one-sided, with Intel granting a li-

cense to all other members, the new agreement is symmetrical: all parties to the agreement grant a license to all other parties for any patents that they or their affiliates hold.

One concern with the prior agreement was that it applied only to a specific version of the specification, in that case 1.0. The new agreement covers future versions as well, but it allows participants to exempt patents that would apply only to future revisions, provided that the company provides written notice to the group of such intent before the revision is voted on. The group could then choose to modify the specification to avoid infringing the patent. Failure of a participating company to notify the group of patent claims that would affect the revision to the specification would automatically license those patent claims to other members of the group.

Another concern of Intel's was the PCI specification's optional support for a 486-style burst transfer, in which a non-linear address order is used to optimize accesses to 64-bit memory systems. Intel has been granted a patent on this burst technique and was unwilling to give up this weapon against makers of compatible processors. The license agreement specifically exempts this aspect of the specification. Thus, any PCI design that implements this burst order would require an Intel patent license. ♦

