New PA-RISC Processor Decodes MPEG Video

HP's PA-7100LC Uses New Instructions to Eliminate Decoder Chip

by Linley Gwennap

*When the 7100LC was first revealed (see **061504.PDF**), HP discussed the basic design of the chip but remained coy about the multimedia extensions. Now that systems are shipping, the company has agreed to discuss these features of its low-end processor.*

Hewlett-Packard's newest PA-RISC processor, the PA-7100LC, is designed to provide audio- and video-processing abilities superior to those of any other general-purpose CPU. Like the i860 and 88110 before it, the chip includes extensions to the base instruction set that efficiently process the lower-resolution data (8–16 bits) typically used for audio and video. According to HP, if these extensions are "successful," they will be included in future PA-RISC processors as well.

While other vendors have included similar instructions, they were mainly intended to accelerate bit block transfers (bitBLTs) for simple graphics. The 7100LC is the first processor to combine these instruction types with dual integer ALUs and a fast enough clock rate to perform MPEG video decoding in software, eliminating the need for an external video decoder. For many applications, systems using the 7100LC will deliver acceptable video performance without an expensive video subsystem. MIPS Technologies and other processor vendors are working on similar extensions for future products.

Designed for Real-Time Video

When designing the 7100LC, the team had a goal of performing video decoding in real time, but an analysis of MPEG software showed that it requires 200–250 million operations per second (MOPS) to attain the desired frame rate and resolution, far greater than the 50–100 MOPS achievable on most current CPUs. These operations are performed on 8-bit data; each MPEG pixel consists of three 8-bit color values.

Since PA-RISC handles data in 32-bit chunks, most of the data path is wasted when performing 8-bit calculations. The design team realized that performance could be greatly increased by using the wider data path to perform multiple calculations at once. One approach is to perform four 8-bit operations at once, but this technique requires checking for overflow and underflow after each operation and normalizing the results. Instead, HP chose to divide the data path in half.

The new instructions all perform two 16-bit operations per cycle. The added bits provide extra precision for intermediate values of these calculations, eliminating the normalization overhead. HP claims that removing this overhead yields better overall performance than doing four operations per cycle with extra normalization.

The 16-bit (halfword) data size also works well for processing voice-quality audio data. Although CD audio uses 16-bit data, intermediate calculations typically use higher resolution to maintain the signal-to-noise ratio.

While the new instructions double the throughput of the ALU, the 7100LC could not deliver the required speed with a single ALU at its target clock rate of 80 MHz. The designers chose to add a second, independent integer ALU. This structure not only allows the chip to reach its video-processing goals but also significantly improves performance on other integer applications.

With the new design, HP says that an 80-MHz 7100LC can decode MPEG-1 video, with no sound, at 30 frames per second (fps) using CIF (352×288) resolution. When processing the full MPEG-1 data stream, the chip can display video at 27 fps with monaural sound or 25 fps with full stereo sound. The 60-MHz version delivers about 20% lower frame rates.

New Instructions Speed 16-Bit Data

The most common MPEG calculations are addition, subtraction, and multiplication. The last case usually involves multiplication by a constant; the discrete cosine transform (DCT) calculation, a major component of MPEG, contains no variable multiplication.

In the 7100LC, the PA-RISC ADD, SUB, and SHnADD instructions have new variants that operate on two halfwords at a time. In hardware, this simply requires disabling carry propagation from the lower halfword to the upper halfword. Like their predecessors, the new variants are three-operand instructions ($R1 \otimes R2 \rightarrow R3$).

The basic SHnADD instruction shifts a 32-bit value left by one, two, or three bits and adds the result to a second 32-bit value. Just one or two of these instructions can multiply a value by a small constant. The new variants can multiply two 16-bit values by any 8-bit constant with a sequence of no more than three instructions. Unlike the base instruction, the halfword SHnADD allows right shifts of up to three bits, allowing values to be divided by small constants as well.

A new instruction performs an arithmetic mean of two values (actually, two pairs of 16-bit values). In hardware, this is a simple addition followed by a one-bit right shift. This instruction is used when processing MPEG "B" frames *(see **060804.PDF**)*, which combine data from two other frames. It is also useful for color interpolation

and anti-aliasing, particularly when expanding an image to simulate higher resolution.

Like their parent instructions, the new variants are available in signed and unsigned versions. Signed arithmetic is frequently used when deciphering MPEG "P" and "B" frames, which encode data as the signed difference between the current frame and one or two others.

The new instructions all provide an option for saturation arithmetic; in this mode, an overflow or underflow returns the highest or lowest possible value (respectively) instead of simply wrapping around. This is useful when combining pixel intensities; for example, two bright colors should combine as white if their digital values add to more than the brightest possible value. Saturation arithmetic is also used in audio processing.

The design team was careful not to adversely affect either the die area or cycle time of the 7100LC by adding these extensions. The circuit changes consisted of a small amount of control logic and a few multiplexers; HP estimates that this circuitry occupies 0.04 mm^2 and uses what otherwise would have been empty areas. While some of the multiplexers, particularly for the saturation arithmetic, are in the main data path, this section of the 7100LC is not in the critical timing path and thus does not impact the overall cycle time.

These instruction extensions are product-specific and will not execute on other PA-RISC processors. Although HP is considering adding these instructions to the base instruction set in the future, they will probably continue to be optional, as server products may not need to implement them. On the other hand, it seems unlikely that the company would build a CPU solely for the server sliver of the PA-RISC fragment of the system market, but HP wants to keep its options open.

Video Benefits Depend on Software

HP expects its 7100LC-based systems (see sidebar) to be used for video-based training and other applications using prerecorded material. Although the power of the new chip is impressive, it cannot perform the real-time video encoding required for multimedia authoring or video teleconferencing.

For users to take advantage of the chip's video capability, appropriate software must be available. HP offers, for $99, a package called MPower that runs under its proprietary HP-UX operating system and provides video viewing and other multimedia functions. Other HP-UX applications may eventually incorporate video as well via operating system calls.

The 7100LC's new instructions are not unique; the i860 was the first general-purpose processor to implement byte and halfword operations, and the 88110 recently followed suit. Both provide instructions for adding, shifting, and multiplying pixel data with signed, unsigned, and saturation options; the 88110 even has instructions for packing and unpacking pixels. None of these features prevented these two processors from becoming irrelevant to the general-purpose market due to a lack of system vendors and application software.

To move beyond the technical market, HP must broaden the number of software applications that can take advantage of the 7100LC's video processing; the much-rumored Windows NT port could ultimately let the new processor deliver video to the masses. ♦

7100LC Systems Announced

HP has announced a family of desktop workstations and servers based on the PA-7100LC processor, all available immediately. The most impressive is the Model 712/60, a fully configured workstation for $3,995, cutting the entry price for PA-RISC systems nearly in half. The price includes a 15" color monitor, 16M of memory, and a 240M disk. At 58 SPECint92 and 79 SPECfp92, the 60-MHz system more than doubles the performance of the RSC-based RS/6000 M20 and the microSPARC-based Sun Classic, the only other RISC workstations in this price range. The new system matches the integer performance of a 60-MHz Pentium PC at about the same price, but the RISC system has better I/O capabilities and floating-point performance.

The Model 712/80i runs its 7100LC processor at its full speed of 80 MHz. This raises the integer rating to 84 SPECint92, allowing the $8,800 system to outperform similarly priced workstations based on the PowerPC 601, R4400SC, or Alpha 21064, as well as the fastest Pentium PCs. HP has chosen to cripple the floating-point unit in the 712/80i, however, limiting its SPECfp rating to 79, the same as the 60-MHz system. This restriction keeps the new system from cannibalizing sales of HP's higher-priced PA-7100 workstations.

The 7100LC (unfettered) is also used in new E-series servers, dropping the entry price for a configured PA-RISC server to $7,570 for a 48-MHz system. The company hopes to compete with PC servers by offering its more robust HP-UX operating system while matching the price/performance of 486 and Pentium systems. HP says the new servers will significantly outperform IBM's CISC-based AS/400 systems.

By integrating the memory controller and other system logic, the 7100LC has enabled HP to bring PA-RISC performance to new, low price points. HP's clear leadership in the $4,000 range will pressure its competitors to aggressively price forthcoming systems using the microSPARC-2, Alpha 21066, or R4600 processors.

The new systems will be attractive to customers already using UNIX, but HP will find it difficult to attract customers accustomed to PC operating systems. A native port of Novell Netware is in progress, and HP continues to hint at a Windows NT announcement; these operating systems, coupled with the new low-cost hardware, could let HP compete with Pentium boxes on a more level playing field.

