MICROPROCESSOR REPORT

THE INSIDERS' GUIDE TO MICROPROCESSOR HARDWARE

VOLUME 8 NUMBER 2 FEBRUARY 14, 1994

TI Shows Integrated x86 CPU for Notebooks

"Rio Grande" Includes Memory Control, PCI Interface in Processor

by Linley Gwennap

Aiming to take a bigger bite of the growing notebook market, Texas Instruments has revealed the design of a highly integrated processor, code-named Rio Grande, that is the first x86 processor to include a PCI interface on-chip. The project also includes the first PCI-based system-logic chips designed specifically for notebook systems. Rio Grande will enable the design of lower-cost portable PCs powered by a 66-MHz 486 core.

A recent entrant in the x86 game, TI has exploited Intel's relative weakness in the notebook market to become a significant player, shipping over one million x86 processors last year (not including chips fabricated for one-time partner Cyrix). Almost all were 486SLC/DLC processors, as TI's newer 486SXL family was announced late in the year *(see **071504.PDF**)*; many were used in TI's own Travelmate laptop system.

The Rio Grande processor is based on TI's SXL, which combines Cyrix's 486 CPU core with an 8K write-through cache. The integrated processor adds memory control and a PCI bus interface. The two system chips handle basic I/O and two PCMCIA slots. The company did not announce price or availability of the new chip set; samples could be ready as early as this spring, and production shipments should occur by the end of the year.

Cutting the Cost of Notebook Systems

TI's primary objective was to combine the logic of a typical notebook PC into a smaller number of chips, reducing system size, cost, and power usage. A small, simple chip set also helps system designers get their products to market faster.

Figure 1 (see below) shows that the processor chip combines all high-frequency (>33 MHz) components, eliminating the need to route fast signals on the board. As a bonus, the memory interface can run at 66 MHz instead of 33, as in most systems. A combo chip provides system logic and handles low-speed I/O interfaces, including serial, parallel, and IDE ports. A third chip supports two PCMCIA slots, including hot-insertion buffers. The three chips are connected using a PCI bus.

TI lacks a competitive graphics controller and did not include a graphics chip in Rio Grande. Although many vendors have PCI-based graphics controllers, most are intended for high-end desktop systems; TI expects that notebook-oriented PCI controllers will be available by the time Rio Grande ships.

All three chips operate at 3.3 V or 5 V, as does the PCI bus that connects them. Even at the lower voltage, the CPU will run at 50 or 66 MHz, and the PCI bus can be clocked at up to 33 MHz (one-half of the CPU speed). Either 3.3-V or 5-V DRAMs can be used, and the PCMCIA controller supports cards at either voltage. All three chips in the set are packaged in 208-pin PQFPs.

PCI Replaces CPU Local Bus

The Rio Grande CPU uses the 486SLC core *(see **060501.PDF**)* that TI has licensed from Cyrix. This core has about 20% lower performance than Intel's 486 and thus must be clocked faster for similar throughput. Rio Grande's 8K write-through cache matches the specifications of the cache on Intel's 486. One drawback to the new TI processor is that there is no way to connect an external cache; most notebook systems don't implement this feature, however. It also has no math coprocessor, although a standard x86 coprocessor can be added.

As Figure 2 shows, the integrated memory controller and PCI bridge connect to the CPU through the processor local bus, just as they would if implemented externally. The difference is that this bus is clocked at the full CPU speed rather than at half speed. Unfortunately, the CPU (like the 486SXL) does not implement burst mode on this bus, so a cache line fill takes 360 ns (24 cycles) compared with 300 ns for a 66-MHz 486DX2. According to TI, however, Rio Grande has an advantage on DRAM writes, taking 75 ns per word versus 90 ns for the DX2.

Depending on the mix of read and write transactions, the 66-MHz Rio Grande processor bus should have about the same performance as an Intel 33-MHz 486 bus.

While this does not seem impressive, it means that the faster clock speed, made possible by the fact that the entire CPU local bus is contained in the Rio Grande processor chip, offsets the performance loss caused by the lack of burst-mode transactions. In summary, a 66-MHz Rio Grande should be similar to a 50-MHz DX2 in performance on system-level benchmarks.

Unlike a DX2, the Rio Grande processor requires a full-speed clock input—that is, either 50- or 66-MHz. An on-chip PLL generates an even faster 2×clock for internal timing edges. Although this high-speed clock input may be an annoyance to system makers accustomed to 25- and 33-MHz clocks, it requires only a single, short trace to route the signal.

First PCI Chip Set for Notebooks

The Rio Grande combo chip contains most of the system logic and standard peripherals needed for a simple PC system. Included are:

- A PCI bus arbiter
- A real-time clock with 128 bytes of SRAM
- PC/AT system logic (DMA, interrupts, etc.)
- One serial port, compatible with National 16550
- One Centronics-compatible enhanced parallel port
- A fast IDE (hard disk) interface
- An 82077SL-compatible floppy-disk controller
- XD-bus support for external peripherals

The combo chip does not include a keyboard controller; this must be added externally via the XD-bus.

The combo chip also has a power management unit with six power states that are controlled by a combination of activity timers and software intervention. The chip can monitor the activity of each of the integrated peripherals, the VGA frame buffer, the PCI bus, two off-chip peripherals, and four interrupts (IRQs). The combo chip has a pulse-width-modulated (PWM) output that controls the brightness of the LCD backlight to one of 16 levels. The system can resume processing after a power-down due to a variety of interrupts and alarms.

For system management, the processor implements the Cyrix SMM protocol. All three chips are fully static and draw less than 100 µA when the clock is stopped.

The PCMCIA controller complies with PCMCIA version 2.0 and ExCA 4.1. It is register-compatible with Intel's 82365SL DF. Unlike many PCMCIA controllers, the electrical buffers necessary for hot insertion of cards are integrated. The PCI bus interface assembles 8- or 16-bit data from the cards and transmits it as 32-bit words. For additional expansion, up to four controller chips can be cascaded in a single system.

These two chips are the first PCI-based products announced with basic PC peripherals such as serial, parallel, and IDE ports. Other chip vendors have focused on adding PCI interfaces to high-speed peripherals and providing PCI-to-ISA bridges for slower devices. Although this strategy is fine for desktop systems, the Rio Grande chip set offers the level of integration needed for portable systems while retaining the high performance of PCI. The system-logic chips could be popular for notebooks using other processors, particularly the forthcoming low-voltage Pentium, but TI would prefer to sell them as a set with the Rio Grande processor.

TI Must Keep Costs Low to Be Competitive

The Rio Grande processor will be manufactured in a 0.65-micron, three-layer-metal CMOS process, representing a 10% shrink from the process used for the current 486SXL chips. TI expects the die size to be around 115 mm^2. The processor uses a modular design strategy, with the memory and PCI controllers implemented as gate arrays surrounding the custom CPU core; a fully custom design might have been more compact but would have taken longer to implement.

The MPR Cost Model *(see **071004.PDF**)* estimates that the Rio Grande processor will cost over $50 to build,

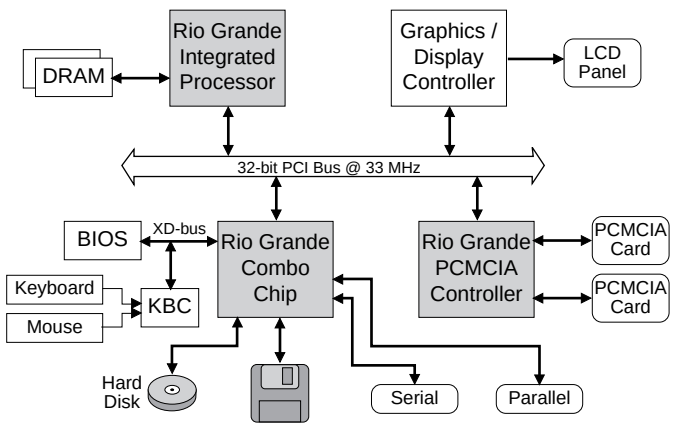

Figure 1. The Rio Grande chip set, plus a PCI graphics chip, contains nearly all the logic needed for a simple notebook computer.

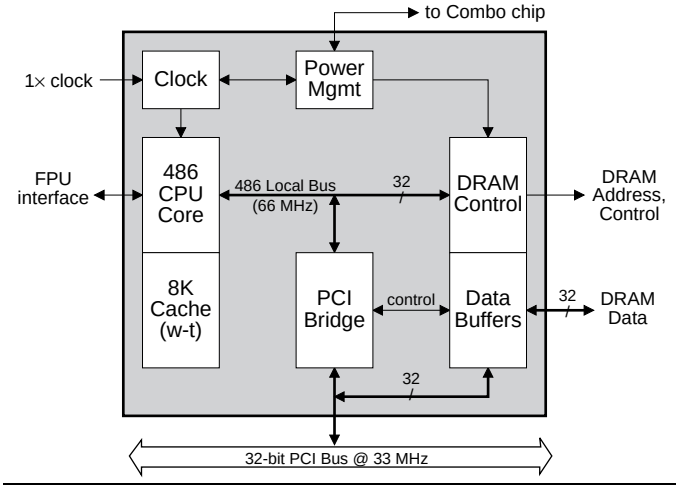

Figure 2. The Rio Grande processor integrates a memory controller and a PCI bus interface, reducing system chip count.

about 20% more than the SXL. Although the more advanced manufacturing process results in a smaller die than the SXL, its higher wafer cost and defect densities drive up the cost. As the process matures, the manufacturing cost of the Rio Grande CPU could drop by 20%.

TI has not announced pricing for the new chips, making it difficult to assess their competitiveness. Rio Grande should handily outperform Intel's fastest part without floating point, the 33-MHz 486SX, which is currently popular in low-cost notebooks and carries a list price of $130. Today's high-end portables rely on faster 486DX2 parts that list for $280 or more.

By the time Rio Grande begins shipping, however, the notebook-processor market will have changed dramatically. Intel plans a rapid decrease in DX2 pricing to make room for its low-voltage, high-performance DX4 parts. Fast SX2 processors will emerge from AMD and Intel, keeping price pressure on products such as Rio Grande. These other processors require chip sets such as VLSI's Scamp IV *(see **070903.PDF**)* to match the system logic of the TI chips; Scamp IV costs about $60 today, but its price will also drop. As a result, the Rio Grande three-chip set will need to be priced around $150 to be competitive.

Another competitive issue for Rio Grande, and TI in general, is customer demand for floating point. TI lacks an x86 FPU and thus cannot easily add this function to Rio Grande. Intel may choose to emphasize the FP performance of its DX2 and DX4 chips and attempt to increase demand for this feature; if so, TI might have to further cut the price of its chips to reflect this deficiency. TI will promote the added integration of its chip set, but it is unlikely that this feature can carry a significant price premium.

486SL Strategy Revisited

Since Intel has abandoned its highly integrated 486SL line, it has left an opening for a more focused player such as TI to step in. Rio Grande could succeed where the 486SL failed for several reasons. First, TI has done a much better job of efficiently integrating memory and bus interfaces onto the processor; Rio Grande's 20% cost premium is much better than the 80% higher manufacturing cost incurred by the 486SL. TI also has lower overall profit margins than Intel and is therefore willing to accept the lower margins associated with system logic. Finally, by choosing to integrate PCI instead of ISA, TI allows system designers to add high-speed peripherals.

One problem for TI is its legal struggle with Cyrix *(see **071702.PDF**)*. Rio Grande, like TI's other x86 products, relies on the 486SLC design licensed from Cyrix—a license that is now under dispute in the courts. If Cyrix prevails in its suit, TI could lose its rights to the SLC core and be forced to remove its products from the market. Given the pace of similar lawsuits, however, it seems unlikely that this would happen before Rio Grande starts shipping, if ever. TI, of course, believes it will retain the rights to the Cyrix core, rendering this speculation moot.

Assuming no sudden adverse legal decisions, Rio Grande should give TI a new, potent weapon with which to attack the notebook market. If the company prices the chip set to match Intel processors and chip sets with similar performance and features, the added integration should be a strong selling point. By stepping into the breach left by the 486SL, TI should be able to expand its x86 market share, perhaps even to the point that Intel will be forced to notice. ♦

Yukon, Ho!

TI also disclosed a few details about the next product in its "Rivers" series, code-named Yukon. It will be a new, higher-performance core still based on the Cyrix 486 CPU. The company did not specify what improvements would be made, but a shrink to 0.5-micron CMOS is in the works, which could boost clock rates to 80 or even 100 MHz at 3.3 V. Other possible improvements would be to expand the cache to 16K, add write-back capability, or add burst transactions to the 486 local bus.

TI expects to begin sampling devices based on the Yukon core by the end of 1994. The new core will be used to improve both the standalone SXL line and the integrated Rio Grande family. Note that the Rio Grande system chips will also work with the more powerful processors if they continue to implement a PCI local bus.

