

PA-7200 Enables Inexpensive MP Systems

HP's Next-Generation PA-RISC Also Contains Unique "Assist" Cache

by Linley Gwennap

Aiming to reinvigorate its PA-RISC processor line, Hewlett-Packard unveiled its PA-7200 design in papers delivered at the ISSCC and Comcon conferences. The new chip will allow HP to compete more effectively against inexpensive multiprocessor (MP) workstations and servers from Sun, which has become the dominant MP vendor. The 7200 will also increase HP's uniprocessor performance, leading the charge against new high-speed CPUs expected from Digital, IBM, and others.

While leveraging heavily from the existing PA-7100 design (see [060406.PDF](#)), the 7200 adds several new features. The chip connects directly to a new 768-Mbyte/s system bus that can connect up to four 7200 chips along with system memory and I/O. Like the PA-7100LC, the 7200 adds a second integer ALU to increase throughput on integer applications. While retaining the off-chip primary caches of previous HP processors, the new design uses prefetching and a small on-chip "assist" cache to improve memory performance. It also adds bi-endian support. The 7200 is manufactured in a new 0.55-micron CMOS process, allowing clock speeds of up to 140 MHz.

As with its previous processors, HP has no plans to market the PA-7200 openly, although it may provide the part to its PA-RISC partners—Convex, in particular, is interested in the 7200 for its parallel systems. HP did not

reveal a price for the forthcoming CPU but said that it would begin shipping in systems by 1Q95. This schedule seems conservative, as the company already has built the first version, which is capable of running operating-system software in a multiprocessor configuration.

Dual Integer Units Improve Throughput

The 7200 is the ninth PA-RISC processor designed by HP; like its predecessors, it uses a simple five-stage pipeline to minimize stalls and interlocks. The only frequent penalties are a one-cycle load-use interlock, a one-cycle mispredicted branch penalty, and a one-cycle penalty for a store followed by a load. HP has eliminated the store-store penalty incurred by previous PA-RISC processors by working with its SRAM vendors to improve the write timing of their standard parts.

Although the 7100 can issue two instructions per cycle, one of the two must be a floating-point operation. The new chip remedies this problem by adding a second integer unit, as Figure 1 shows. Thus, the 7200 can execute two integer instructions per cycle, with some restrictions. Only one integer unit can handle loads, stores, and shifts; these types of instruction cannot be paired with each other but can be paired with simple integer math operations. A branch instruction can be handled by either unit but cannot be paired with its successor, as many branches can conditionally nullify the execution of that instruction.

Like most superscalar processors, the 7200 has few alignment restrictions for instruction pairing, improving performance even on older code that has not been recompiled. To remove resource and dependency checking from the critical path, these functions are performed as instructions are loaded into the cache. Six predecode bits are stored in the cache for every two instructions. The extra bits keep the pipeline flowing smoothly but add a 10% overhead (typically one extra SRAM) to the off-chip instruction cache.

The predecode bits do not fully indicate whether the instructions can be paired; further decoding is done when the instructions enter the pipeline. The extra bits, however, simplify the checking so it does not extend the instruction decode and issue beyond a single clock cycle. Because instructions need not be aligned to be paired, the issue logic may attempt to pair instructions that were originally loaded into the cache as separate doublewords; in this case, the issue logic must check the predecode bits from both doublewords.

The remainder of the processor core is leveraged

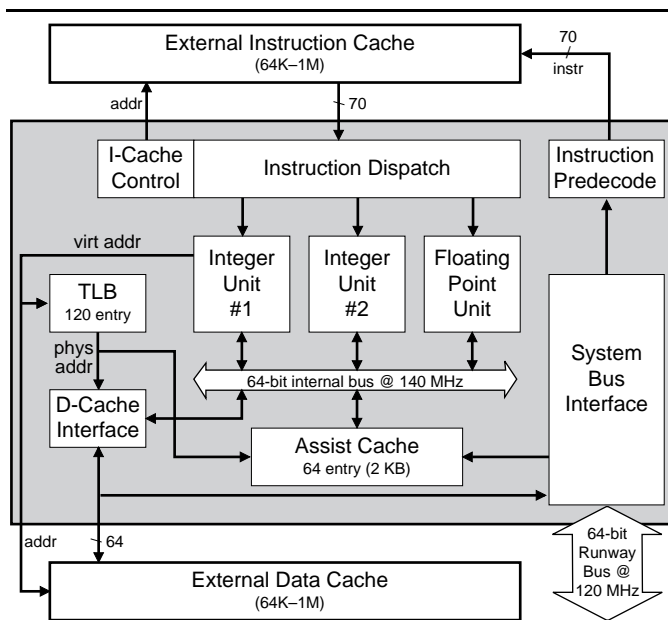


Figure 1. The PA-7200 contains dual integer units and a small "assist" cache but no other on-chip caches.

from the 7100 and simply shrunk for the 0.55-micron process. The floating-point unit, in particular, survives unchanged, retaining its two-cycle latency for addition and multiplication even at the higher clock rate.

Assist Cache Reduces Thrashing

The 7200 retains the off-chip primary caches from previous HP designs. This technique provides single-cycle access to a large cache memory (up to 2M), achieving a better hit rate than small on-chip caches, particularly for applications with large code and data sets. The disadvantage is that it requires extremely fast SRAMs: 6 ns at 140 MHz. HP's experience with this type of design allows it to keep the SRAM access time within one nanosecond of the clock period.

One simplification required by this technique is that the primary cache is direct-mapped; a fast set-associative cache would require far too many pins to implement off-chip. A direct-mapped cache, no matter how large, is subject to thrashing if a program repeatedly accesses two or more different addresses that map to the same physical cache location.

The 7200 implements a 64-entry assist cache that nearly eliminates such thrashing for data accesses. Since the assist cache is fully associative, each entry can back up any 32-byte entry in the primary data cache, or all 64 entries could back up a single primary cache line. This organization is different from a simple two-level cache design because both caches respond in a single cycle and are logically one cache. This design combines the higher associativity attainable by on-chip caches with the large size achieved by an off-chip cache.

The assist cache also acts as a buffer between main memory and the primary cache. Data from memory is first loaded into the on-chip assist cache before moving to the external cache using a FIFO (first in, first out) order. This reduces the overhead of moving the data into the cache, since a new cache line from memory can be moved into the assist cache in a single cycle without interfering with accesses to the off-chip cache. In contrast, the 7100 requires four cycles to move a line into the primary cache, preventing any cache reads during this period.

To improve the hit rate, loads can carry a new "hint" that tells the chip not to move data to the off-chip cache but instead return it directly to main memory. This hint is useful for data that will be used only once, preventing it from polluting the primary cache.

Although the off-chip data cache is virtually indexed, allowing an access to be launched with minimal overhead, the assist cache is physically indexed. For each cache access, the virtual address must be translated by the TLB, and the resulting address is used to access the assist cache—all in a single cycle. Since both the TLB and the assist cache are on-chip, this is not a critical timing path, and the physical indexing eliminates aliasing

problems and reduces the size of the tag array.

Despite the new assist cache, the continued reliance on off-chip caches is the limiting factor for the performance of the 7200. The obvious effect is the critical path through the external SRAMs; the chip could probably run at a higher clock rate if faster SRAMs become available, but even 6-ns parts will be hard to find and expensive. The 64-bit interface to the external instruction cache also limits the 7200 to issuing two instructions per cycle. To match the performance of its competitors, HP must move to four (or more) instructions per cycle, requiring either a 128-bit instruction-cache interface (on top of the 64-bit data-cache bus) or an on-chip instruction cache.

Prefetching Reduces Memory Overhead

The new design implements an aggressive set of prefetch mechanisms to reduce apparent memory latency. These mechanisms combine hardware and software control to initiate memory accesses before the data is needed. If successful, cache miss overhead can be hidden and execution can continue with no penalty. If unsuccessful, prefetching can bring unneeded data into the cache, replacing more valuable information, and may even interfere with fetches of needed data.

The 7200 has a fairly simple instruction prefetch mechanism. On an instruction cache miss, the subsequent line is immediately prefetched after the missing line is fetched. When a prefetched line is accessed for the first time, the next sequential line is then prefetched, even if another prefetch is still in progress. This algorithm results in significant performance improvements when executing long, linear code sequences. Instruction prefetching can be disabled for programs with short routines and frequent branches.

Data prefetching can be initiated by software using a prefetch (load to register zero) instruction. The 7200 will also prefetch data when address modification is used. For example, the PA-RISC instruction:

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LDWX,m R1(R2), R3
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loads the value at the address contained in R2 into R3, then adds R1 to R2 (post-increment). When the 7200 encounters this instruction, it speculates that the instruction is part of a loop and prefetches data from the new address contained in R2. This algorithm allows the processor to determine both the stride and direction of the data references. Up to four prefetches can be outstanding, allowing the CPU to prefetch along four different data streams or to get further ahead of a single stream of references.

Runway Bus Boosts Bandwidth

HP has replaced the old, proprietary system bus from the 7100 with a new, proprietary system bus called Runway, more than tripling the total bandwidth from the previous part. Runway is a 120-MHz (maximum) 64-

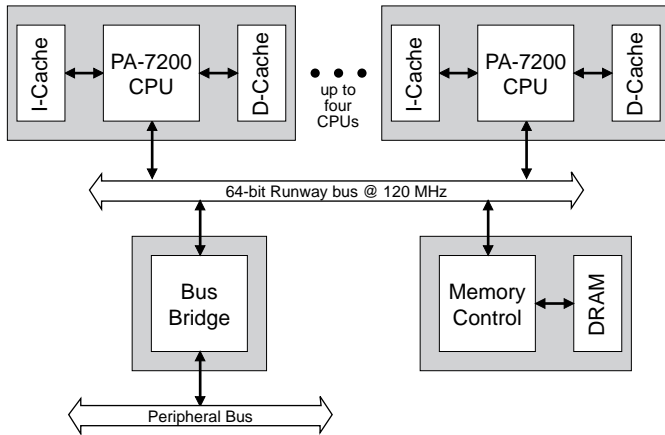


Figure 2. The Runway bus allows several PA-7200 processors to be connected without any buffers or glue logic.

bit bus that multiplexes address and data. It uses a split-transaction protocol, allowing up to six transactions (per processor) to be in progress at once. Overlapping the transactions keeps the bus utilized even during memory latency. Because the CPU can run faster than 120 MHz, the 7200 supports ratios of 1:1, 3:2, and 4:3 between the CPU and bus clock frequencies.

Bus arbitration is performed in parallel with data transfers, using a separate set of signals. There is no central bus arbiter; each device contains its own arbitration unit, simplifying the arbitration process but increasing the complexity of each device on the bus. Another set of signals carries an ID code for each transaction, allowing devices to immediately recognize return data, even when multiple transactions are in progress. The only overhead

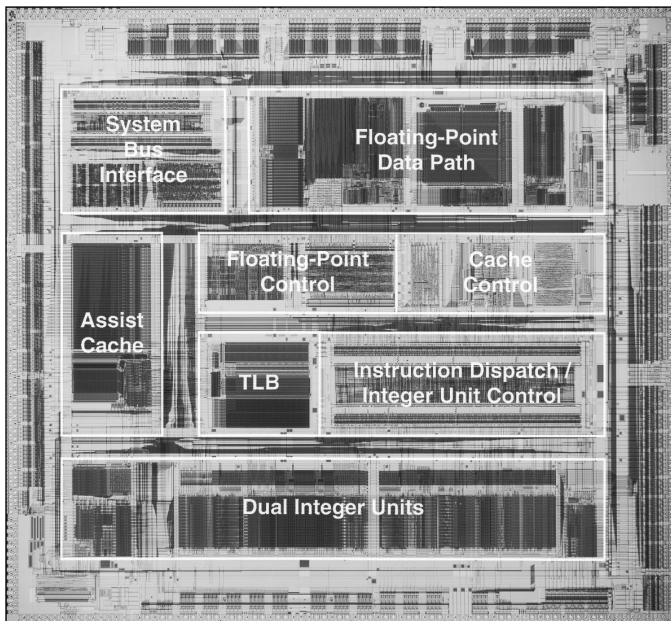


Figure 3. The PA-7200 die measures 14 x 15 mm and contains 1.26 million transistors using a 0.55-micron CMOS process.

on the multiplexed address/data bus is a single address cycle for every four data cycles, resulting in a sustainable bandwidth of 768 Mbytes/s.

Runway supports multiple processors with no glue logic: up to four 7200 chips can be connected directly. The bus supports cache-coherency checks to ensure that data is kept up to date in systems with multiple processors. Each processor snoops all Runway transactions; if an address hits a dirty line in the processor's local cache, the CPU responds by sending that data directly to the requesting CPU. The memory controller uses the same data to update main memory, eliminating the need to place it on the bus twice.

Figure 2 shows how a low-cost multiprocessor system could be built using the 7200. Each processor module contains a single 7200 chip and cache memory; no additional interface chips are needed to connect multiple processors. HP estimates that the Runway bandwidth is sufficient for up to four 7200 processors without significant degradation.

This configuration is, not coincidentally, similar to that used in Sun's successful SparcStation 10. Sun's system uses the SuperSparc chip, which contains a direct interface to MBus; up to four processors can be connected to a single MBus. SuperSparc cannot control an external cache, however, so most SuperSparc modules contain an extra cache-control chip, increasing the cost.

MBus also offers far less bandwidth than Runway. The peak bandwidth of MBus is 320 Mbytes/s, but the Sun design can handle only one transaction at a time, forcing all devices to wait during memory or I/O latency. Thus, the sustainable bandwidth can be 120 Mbytes/s or less, depending on the speed of the memory system (see MPR 8/8/91, p.8). A Runway-based system will have more than six times that bandwidth, making it better suited for multiple high-performance processors. This bandwidth is even greater than that of Sun's high-end XDBus (see [070301.PDF](#)).

New Package, Process Increase Cost

The 7200 is the first PA-RISC chip to take advantage of HP's new 0.55-micron, three-layer-metal CMOS process, which was codeveloped with Analog Devices. This process offers a significant improvement in speed and density over the 0.8-micron process used for the 7100 and 7100LC.

The new process is optimized for operation at the unusual level of 4.4 V. This voltage is a compromise; the 120-Angstrom gate oxide of the new process cannot tolerate 5-V operation, but a move to 3.3 V would have reduced the transistor speed. The external I/O operates at 3.3 V to reduce signal swings and thus the transmission times to the fast SRAMs and the Runway bus.

The increased density allows the company to pack the second integer unit, the 2-Kbyte assist cache, and the

more complex bus interface onto the 210-mm² die shown in Figure 3. The MPR Cost Model (*see 071004.PDF*) estimates that the 7200 will cost about \$280 to manufacture, nearly twice as much as its predecessor. Since the 7200 die is only slightly larger than the 7100, the increase is primarily due to the higher wafer cost and initial defect density of the new 0.55-micron process; as the process matures, the cost of building the 7200 could drop closer to \$200.

The manufacturing cost is not helped by the 7200's enormous package, a 540-pin PGA. The chip must also bear a hefty heat sink—it dissipates 29 W (maximum) at 140 MHz. Since HP's current systems are designed to cool the 22-W 7100, it shouldn't take many changes to handle the hotter 7200.

Performance May Lag Competition

HP has not released any measured performance numbers and will not even confirm that the production version of the 7200 will meet the 140-MHz goal outlined in the ISSCC paper. The frequency goal seems reasonable; HP recently announced (*see 0717MSB.PDF*) a slightly improved version of the PA-7100, dubbed the PA-7150, that will run at 125 MHz using the old 0.8-micron process. The new process should provide enough of a speed boost to get to 140 MHz, although HP is still characterizing the part.

HP says that the 125-MHz 7150 will achieve more than 135 SPECint92. Since the 7200 has the same large single-cycle cache, its performance should scale with the slightly higher clock speed. The second integer unit should deliver at least a 10–20% improvement on integer code, but the assist cache probably will not help SPECint92 performance. Combining these factors, we estimate that the 7200 should reach 180 SPECint92 or so.

Performance on SPECfp92 should also scale with frequency. The assist cache and the fast Runway bus will increase performance significantly on some of the FP benchmarks with large data sets, so the 7200 should deliver more than 250 SPECfp92.

Several other RISC vendors plan to deliver new high-end processors early next year. These include the MIPS T5, PowerPC 620, Digital 21164, and Sun's UltraSparc. Although none of these vendors has released specific information about these forthcoming chips, all are claiming greater than 200 SPECint92. To achieve this level of performance, these other processors will execute more instructions per cycle (four to six, peak) and use techniques such as dynamic branch prediction, speculative and out-of-order execution, and higher clock speeds—none of which is present in the 7200.

HP's new chip appears to be slightly ahead of these other projects in time, so it could have a small window as the best-performing CPU before being swamped in 1995.

Price and Availability

HP has no plans to sell the PA-7200 on the open market but will provide it to members of the Precision RISC Organization (PRO). The company has not announced a price for the part. It says that volume shipments will begin in 1Q95. For more information on PRO, call 408.447.4249. For more information on the PA-7200, contact Cindi Fino-Cooper at 408.447.5551.

In the short term, its chief competitor will be Digital's 275-MHz 21064A, which that company rates at 170 SPECint92 and 290 SPECfp92. Digital is already sampling the 21064A and plans to begin volume production in 3Q94, well before the 7200.

7200 Excels on Larger Applications

HP claims that the strength of the 7200 is not shown in small benchmarks such as the SPEC92 suite. These benchmarks mostly fit in the chip's large primary cache and do not take advantage of either the assist cache or the high-bandwidth Runway bus. Applications such as on-line transaction processing (OLTP) and scientific programs with large data sets should see more of a performance boost from these features. The aggressive prefetching should also benefit these applications.

The 768-Mbytes/s Runway delivers more than twice the bandwidth of similar memory buses used in the R4400, SuperSparc, and similar processors. The 21064 uses an external bus with more than 1 Gbyte/s of peak bandwidth, but this bandwidth is shared between cache and main memory. Only IBM's Power2 and the MIPS TFP, both expensive multichip processors, have greater memory bandwidth than the 7200. It remains to be seen, however, how the next-generation chips from HP's competitors attack the memory-bandwidth problem.

Given the company's aggressiveness with previous processors, it is surprising that HP is the last of the major CPU vendors to move beyond a 0.8-micron manufacturing process. The company is also slow in implementing the aggressive superscalar techniques expected from other RISC vendors in 1995; HP has a similar design, the PA-8000, that is not due until 1996. These delays may be signs of the company's inability to invest at the pace of other, more broadly used architectures.

Even with these limitations, the PA-7200, coupled with the PA-7150, give HP a solid one-two punch that will re-establish it among the performance leaders. The low-cost MP capabilities of the 7200 will provide an effective counter against Sun's multiprocessor systems. HP has proven adept at creating a broad, successful product line from its PA-RISC processors, and the new chips should allow it to continue to do well in the workstation and server markets. ♦