Motorola Introduces Heir to 68000 Line

Multi-issue 68060 Maintains Upward Compatibility

by Curtis P. Feigel

Eighteen months after describing the architecture, Motorola has formally introduced its line of processors based on the 68060. The new core achieves 90 Dhrystone MIPS at 50 MHz, making it the highest-performance CPU in the 68000 family. It is a superscalar device with some RISC-like implementation techniques, but it maintains binary compatibility with the 68000 family of CISC processors. Although not a drop-in replacement for the 68040, the 68060's pinout and bus are compatible with its predecessor's, making the faster chip attractive both in new designs and as an upgrade to existing machines.

Initial devices will run at 50 MHz, with production quantities of 66-MHz units promised for late in 4Q94. Along with the full-scale processor, the company introduced two lower-cost variants: the 68LC060 (which lacks an FPU) and the 68EC060 (which has neither an FPU nor an MMU).

Even though the '060 represents a major advance over its predecessor, it is too little and too late to save the desktop market for Motorola. From a strong position in the mid-1980s—with design wins at Apple, HP, and in other workstations—the 68000 family's use in new desktop designs has dwindled to virtually zero. Desktop system vendors have abandoned the Motorola line because of the company's difficulties in delivering the 68040 and that chip's lack of competitive performance. With the desktop out of reach, Motorola is focusing on the embedded-systems market, an arena that it dominates with its midrange processors.

The new chips further expand Motorola's already broad 68000 line, which includes numerous versions of its 32-bit processors integrated with high-performance peripherals for communications, automotive, printer, and other embedded applications. In engineering the '060, Motorola employed a flexible, modular design process that will simplify removal and addition of major function blocks. The company can make varying price/performance tradeoffs to generate a spectrum of processors that execute the same instruction set.

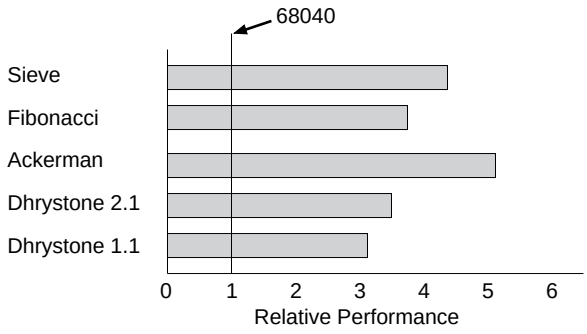

Figure 1. On small, compute-intensive benchmarks, the 50-MHz 68060 delivers much better performance than the 25-MHz 68040. These tests compared systems with the same processor-bus speed and no second-level cache. (Source: Motorola)

Big Step Skips '050

Motorola's goal for the '060 was to achieve a performance gain of 1.6 over the '040 through architectural improvements alone. Although the company planned a 68050 device at one time, that design incorporated only minor enhancements, such as larger caches, to the '040. Discussions with customers convinced Motorola to skip the '050 and devote its resources to making the major architectural step of the '060. To optimize the new design, the company performed a "dusty deck" study of existing applications, looking specifically at ways to improve the hardware for typical conditions.

Motorola deemed binary compatibility with previous 68000 chips to be a must. Like most superscalar processors, however, the 68060 achieves optimal performance only on recompiled code. Working with Motorola, Diab Data (Foster City, Calif.) has developed an optimizing C compiler for the 68060 architecture.

Projections indicate that, on real applications, the '060 will show a 60% gain over an '040 of the same external clock speed. (Comparing in this manner eliminates the external memory system as a variable.) On SPECint92, for example, Motorola projects that the 50-MHz '060 will be rated at 49, compared with about 25 for a 25-MHz '040. For smaller benchmarks, the gain can be much greater: Figure 1 shows a range of 3.1 to 5.1 times the performance of a 25-MHz '040.

Tests also showed that a 50-MHz '060 had 2.1 times the performance of a 40-MHz '040 running the Macintosh Speedometer benchmark; the 66-MHz version achieved a rating 2.8 times the '040. These figures are from alpha-test sites using actual '060 silicon installed in converted Macintosh machines and in Motorola's IDP (Integrated Development Platform) evaluation boards.

Dual Pipes Improve Upon '040

Motorola described the architecture of the '060 at the 1992 Microprocessor Forum *(see **061505.PDF**)*. As Figure 2 shows, the new superscalar CISC processor employs separate data and instruction caches; each is 8K in size and four-way set associative. The data cache is four-

way interleaved and can support simultaneous accesses to separate banks. Software can freeze either cache, or one-half of either cache, preventing updates on cache misses and ensuring that critical code remains in the cache. The half not frozen acts as a 4K, two-way cache.

The MMU has separate 64-entry data and instruction TLBs that also can each be frozen. Memory management is speeded and simplified by dedicated page-table-walking hardware. The processor also has two TTRs (transparent translation registers) each for data and instructions and an underlying default TTR. These registers provide limited memory-management functions for large blocks of address space without performing a tablewalk. They can be used even when the MMU is frozen or absent (as in the ’EC060).

For the ’060, Motorola has created the PLPA instruction, which can store directly to a physical address, translate to a virtual address on a TLB/TTR hit, or tablewalk on a miss to update the TLB. This combination of features gives programmers a range of memory-management options from simple to sophisticated.

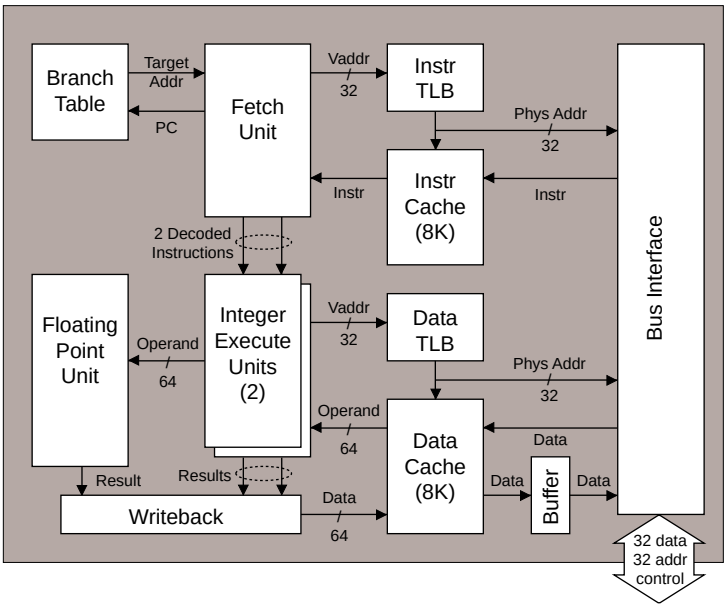

Figure 2. Dual integer pipelines and larger caches distinguish the ’060 from its predecessor. The processor is completely hardwired and uses no microcode.

The 68060’s fetch unit operates autonomously, decoding the variable-length instructions enough to separate them and place each in its own entry in the instruction buffer. The buffer feeds instructions, either singly or in pairs, into dual integer-execution units that are similar to the single unit in the ’040. The pipelines operate synchronously: instructions, including reads and writes, execute strictly in order, with the primary pipeline logically completing before the secondary pipeline.

The units are not identical: the secondary unit cannot execute some types of instructions, and all floating-point instructions must travel down the primary pipeline to reach the floating-point unit. The chip reaches its peak speed of 250 native MIPS when simultaneously executing two integer instructions, each with an embedded load or store, and one branch.

The floating-point unit contains separate add, multiply, and divide/square-root units, although adds and multiplies cannot occur simultaneously. Internally, all floating-point operations are performed in 80-bit extended precision. Complex or infrequently used operations from the ’040 instruction set are implemented via software emulation. The floating-point unit can be disabled, in which case floating-point instructions trap to the F-Line handler, making a full ’060 operate like an ’LC060 or ’EC060.

A four-entry write buffer decouples the processor from the external memory system. According to Motorola, the 68060’s write performance degrades less than half as much as the 68040’s does when comparing write-back to write-through mode.

Because power dissipation is of increasing concern in many embedded designs, Motorola paid special attention to it in the 68060. The 3.3-V supply reduces power consumption by 40–60% from a 5-V supply. The ’060 is a fully static design; the CPU clock can be slowed or even stopped to trade off power for performance. The ’060 also includes a new LPSTOP instruction that halts execution and puts the processor into a low-power mode.

Simplified Bus Cuts System Cost

The ’060 is a more RISC-like design than its predecessor. For one thing, its completely hardwired design uses no microcode. For another, the ’060 is a “restart” machine. In the ’040 “continuation” model, when a trap occurs, most of the processor’s state is saved in a large stack frame. Once that trap is handled, the state of the processor is restored by reloading the pipeline, so execution of instructions in the pipeline can resume where it left off. In the ’060, much less of the processor’s state is saved; once a trap is handled, the unexecuted instructions must be fed into the pipeline and operated on from the beginning. The advantage is a smaller stack frame that offers reduced latency in handling traps, bringing an overall performance gain.

The new processor’s bus protocol is compatible with the ’040, so it can work with existing designs. But the 68060’s bus has more relaxed timing, allowing for slower and less costly external memory and logic. The processor also preconditions data bus lines that are high by driving them to Vcc, making it easier to drive them low if necessary (lines that are low are unaffected). Reportedly, this saves 2 ns over the time required to handle full-swing

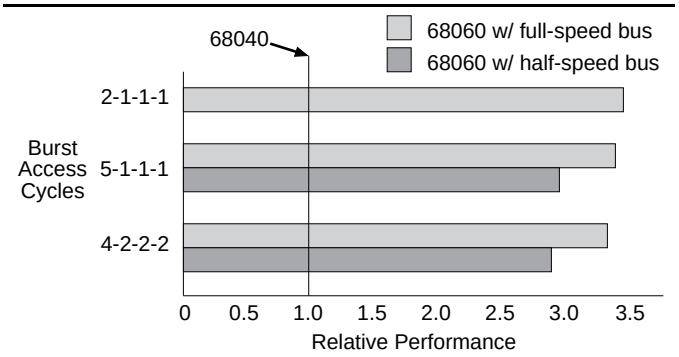

Figure 3. The 68060's write buffer and large caches allow it to maintain performance levels even with wait states. (Source: Motorola)

5-V signals. Figure 3 shows that the '060 maintains its speed advantage over the '040 for memory systems with a variety of wait states. This can result in reduced system cost if the designer takes advantage of it.

A further difference is that the 68060 needs only a 1× clock with 45%/55% duty cycle. It contains neither fussy clock-doubling circuitry nor a phase-locked loop. Its bus implements a fully synchronous protocol based on the rising edge of the clock. The CLKEN signal lets external system logic determine which clock edges are used to identify valid data, allowing half- and quarter-speed external buses—or even a mixed-speed bus. Also, the 68060's bus snooping is simpler than the 68040's: rather than output data when an external master causes a snoop hit, it invalidates the snooped entry in its own cache. This method simplifies the circuitry and still maintains coherency in systems with DMA and in multiprocessor applications.

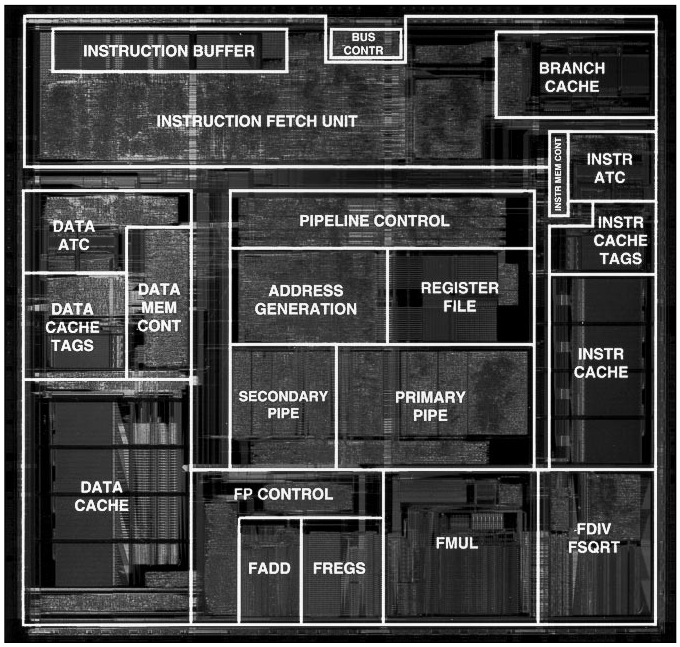

Figure 4. Die photo of the 68060's 2.5 million transistors. Built in Motorola's 0.5-micron CMOS process, the die measures 198 mm^2.

Designed with Upgrades in Mind

The '060 provides a significant performance boost for 68000-family systems. With its binary compatibility, it is the logical choice to upgrade existing '040 machines. The pinout of the 68060's 223-pin PGA is even compatible with the 68040's 179-pin PGA pinout: extra pins are placed on inner rows near the cavity.

Because it is built in a 0.5-micron process, however, the '060 requires a 3.3-V power supply; it cannot simply be dropped into an existing system. Its I/O circuitry is 5-V tolerant (outputs swing between ground and 3.3 V, while inputs are allowed to swing up to 5 V), simplifying the interface to standard PLDs, bus transceivers, and other system logic. This 5-V I/O compatibility makes it possible to design a system with a single socket that will accept either an '040 or an '060.

Initially, Motorola will produce '060s, 'LC060s, and 'EC060s from the same die. This strategy reduces the cost of manufacturing a fully functional '060, as dice with defective FPUs and MMUs can be sold as LC or EC versions instead of being discarded. Assuming that all these defective chips can be sold, the MPR Cost Model *(see **071004.PDF**)* estimates that the 68060 will cost about $120 to build. Note that, in this scenario, all three versions have the same manufacturing cost.

As shown in Figure 4, the FPU and MMU occupy a relatively small portion of the chip, so the number of fully functional '060s will be much higher than the LC and EC versions. If the '060 succeeds in the embedded market, however, the EC version will have the greatest demand. Ultimately, Motorola will reduce its manufacturing costs by designing a new, smaller EC die with no FPU or MMU. Even in this situation, the cost of the full 68060 remains lower, since defective parts can still be used to supplement production of the EC. As the 0.5-micron process matures and a smaller die is used, the manufacturing cost of the EC could drop to $75.

Motorola Loses Desktop Market

The 68060 was originally conceived as a desktop upgrade for Apple, HP, and other 68040-based system vendors. Many of the workstation vendors were already flirting with high-speed RISC chips, however, and production problems with the 68040 (see "Garden Path" sidebar) killed its prospects in this performance-sensitive area. Apple was also hurt by the '040 debacle but retained its faith in Motorola.

The 68000 line has had an intense rivalry with Intel's x86 ever since IBM spurned Motorola for its first PC. Each processor generation has been lined up against its rival in performance. The 68040 delivers performance similar to the 486 running at the same clock speed. The weakness of the '040 is that Motorola struggled to ship 33-MHz parts even as Intel was boosting the 486 to 50

	68060	68040	PPC601	P54C	i960CF
Clock	50 MHz	40 MHz	66 MHz	100 MHz	40 MHz
Instruction Cache	8K	4K	32K	8K	4K
Data Cache	8K	4K	Unified	8K	1K
Data Bus	32 bit	32 bit	64 bit	64 bit	32 bit
SPECint92	49*	35	75	100	N/A
SPECfp92	N/A	23	91	81	N/A
Dhrystone MIPS	90	43.8	N/A	138	62
Price (1,000s)	$308	$218	$370	$995	$198
$/SPECint	6.2	6.2	4.9	9.9	N/A
Transistors (million)	2.5	1.2	2.8	3.3	0.9
Die Size	198 mm^2	164 mm^2	121 mm^2	163 mm^2	125 mm^2
IC Process	0.5 µ, 3M	0.8 µ, 3M	0.6 µ, 5M	0.6 µ, 4M	0.8 µ, 2M
Mfg. Cost (est.) †	$120	$65	$70	$150	$50

Table 1. The new 68060 offers a 50% performance increase over the fastest 68040, but it is significantly slower than PowerPC or Pentium processors. The ’060 delivers better price/performance than Pentium but is beaten by PowerPC. *based on simulation. (Source: vendors except †MPR Cost Model)

MHz and beyond. This performance gap made Apple’s Macintoshes uncompetitive with 486-based PCs and drove Apple to adopt the PowerPC architecture. Companies like Apple and HP knew about the 68060 far in advance of its debut but chose to switch to RISC.

The latest announcement shows the wisdom of this move. As Table 1 shows, the 68060 delivers the same SPECint92 per MHz as Pentium but, at 50 MHz, offers exactly half the clock speed of the x86 processor. The 68060 offers a much lower price than Pentium, but Apple would have been at a significant performance disadvantage had it stayed with the 680x0. The PowerPC 601 offers both better performance and better price/performance than the 68060; a 100-MHz 601 (not shown in the table) will outrun even the fastest Pentium.

This leaves the ’060 with few opportunities on the desktop. Apple has declined to develop an ’060 upgrade card for the large installed base of ’040 Macintosh machines. Third-party vendors will provide ’060 upgrade cards for the Macintosh, but given the new CPU’s $308 list price, such a card would have to sell for $600 or more. Apple has announced PowerPC upgrade cards priced at $699 *(see **080401.PDF**)* with better performance than an ’060 can provide, so most Mac users will follow the company’s lead into the realm of RISC unless they depend heavily on 680x0 software that has not been ported to PowerPC.

Embedded Systems Are Strong Suit

Motorola’s 68000 family has a secure position as the 32-bit microprocessor of choice in embedded systems. Its closest competitor, the i960 family, captures only a fraction of the number of sockets. The fastest i960 processor, the new 40-MHz i960CF *(see **0803MSB.PDF**)*, may seem a viable contender: it delivers two-thirds the 68060’s performance at two-thirds the price. Although Motorola hasn’t integrated peripherals into its high-end processors as it has for its low-end processors, it claims it will do so with the ’060.

The long-lived 68000 family has also spawned its own industry of software, hardware, debugging, simulating, and emulation tools. The ’060 JTAG interface offers a powerful set of features that simplify the process of debugging. It allows external logic to halt and restart the CPU and override processor configuration. Users can also force nonpipelined operation, that is, cause instructions (or pairs) to be dispatched singly and execute completely from issue to retire. The emulator mode disables the branch cache; instructions can then be entered via the pipeline’s debug interface or via trace, breakpoint, or reset exceptions. The interface can also disable all the chip’s inputs and force all its bus outputs to a high-impedance state—handy for checking system logic and for debugging other masters sharing the same bus.

The ’060 was designed from the beginning as a modular processor. It can be stripped down or enhanced in various ways to meet price and performance needs. Versions proposed within Motorola, but not guaranteed to be put into production, include:

- 68060Lite—single integer pipeline, no FPU, cache sizes reduced, similar to 68LC040 but less costly.
- 68060S—instruction set reduced but still compatible with 68000, smaller caches, may integrate customer-specific logic.
- 68060+—undisclosed architectural enhancements

Down The Garden Path

Although Motorola has yet to begin shipments of the 50-MHz 68060, the company is already claiming that the chip will reach 66 MHz by the end of this year, just one quarter after 50-MHz shipments begin. Unfortunately, the company has a poor track record of meeting such claims, as shown by this brief history of the 68040.

4/89—68040 preannounced two weeks before Intel announces 486. Formal ’040 introduction set for 3Q89.

10/89—Company discloses ’040 architecture.

12/89—Motorola admits “No ’040 in ’89.”

1/90—’040 formally announced, general sampling slated for end of 1Q90.

4/90—Company claims ’040 on schedule for volume production midyear. Sample date slips.

9/90—Motorola announces it has begun general sampling of ’040 with volume shipments to begin in October.

11/90—Company claims 1,000 ’040s shipped this month and that volume production has begun.

1/91—HP begins shipping 25-MHz ’040 systems, promises 33 MHz in 2Q91. Benchmarks of new systems fall short of Motorola’s original claims.

6/91—Motorola says 33-MHz parts in September.

6/92—Volume shipments of 33-MHz parts begin. Motorola promises 40-MHz 68040 for September.

12/92—40-MHz parts begin to ship in volume.

that increase performance 20–30% independent of clock frequency.

Process improvements will bring further speed gains and, perhaps more important, cost reduction.

Opportunities Abound in Outworld Colonies

New embedded systems, and existing 68000-family ones, will offer a much bigger opportunity for the ’060. By design, the ’060 is eminently suited to this application. Programmers will appreciate its cache-freeze function. It incorporates power management, and its 32-bit bus is less expensive than 64-bit types. The smaller code size of its CISC architecture requires less RAM, and its write buffer allows for reduced external bandwidth, all of which translates into a less expensive memory system. Still, its price places it at the very high end of this market and it remains to be seen what applications can justify the 68060’s cost.

The trend in embedded systems is toward integration. As Motorola well knows, the most popular processors are the ones that incorporate exactly the peripherals needed for a particular application. This reduces parts count, board space, power consumption, and cost; it also increases reliability and shortens time to market. Motorola has a history of working with embedded-systems developers to integrate the peripherals they need with 68000-family processors. The modular design of the ’060 means Motorola can thoroughly cover the range of performance required for embedded systems, if not for desktop systems.

When Intel promised the Pentium, users allocated space on many desktops well before the chip was available. The ’060, even though available, is a chip with few desktops to land on. ♦

Price & Availability

The 50-MHz 68060, 68LC060, and 68EC060 are now sampling to selected beta sites. General samples will be available 3Q94, with production to follow late in that quarter. Prices are $263, $169, and $150, respectively, in 10,000-unit quantities. Production quantities of the 66-MHz 68060 will be available late in 4Q94, according to the company; no price has been announced. For further information, contact Motorola at 512.891.2917.

