Motorola Chip Combines 68000 with DSP

68356 Communications Engine Integrates 68302 and 56002

by Linley Gwennap

Setting a new level of integration, Motorola's 68356 is the first product to combine a 32-bit general-purpose CPU with a full-featured DSP core on a single chip. Along with the 68000 CPU and 56002 DSP cores, the chip also contains more than 32K of RAM, an extensive set of peripherals, and an autonomous I/O processor. Even with all these features, the newest member of the 68300 family sells for just $65. The chip is designed as a communications interface for portable products, particularly in PCMCIA modem cards, although it can serve in a number of applications.

The 68000 is Motorola's entry-level 32-bit CPU; it runs at up to 20 MHz in the 68356 using a 3.3-V supply, delivering 3.3 Dhrystone MIPS. The 56002 core, using a separate clock, can operate at 45 MHz at that voltage, executing 27.5 peak native MIPS. With a 5-V supply, the CPU can reach 25 MHz while the DSP hits 60 MHz. The combination of these two processors should provide enough horsepower for many high-speed communications applications.

The chip includes a PCMCIA slave interface, so it can be used as the controller in a PCMCIA card without any interface logic. The built-in serial ports are ideal for modem applications up to 28.8 kbps; the DSP can perform filtering and modulation while the CPU manages the modem protocol.

The 68356 also can be used for wireless communications, either as a PCMCIA card or built into the host device. In particular, the chip can process cellular digital packet data (CDPD) and other standards for data transfer over enhanced cellular phone links. A laptop computer or PDA could use a single 68356 chip to provide both wireless and wire-line modem functions.

Multimedia systems could also make use of this device to perform sound processing or audio compression in addition to modem functions. The CPU/DSP combination allows for fully autonomous execution of these functions, although many systems may rely on their main CPU for control and use a less expensive DSP chip.

Line-powered systems that already have an embedded CPU and a DSP (many fax machines, for example) may find the integration of the 68356 appealing. In general, however, the major attraction of the new chip is reduced footprint and lower power consumption; the cost is similar to that of a discrete solution. Thus, the bulk of the design wins should come in portable systems that require small size and low power.

Multiprocessor on a Chip

The new design exemplifies the trend of combining multiple processors of different types on a single die *(see **080605.PDF**)*. Motorola began with the 68302 design (see MPR 10/89, p. 1) and added a standard 56002 core, as Figure 1 shows. The 68356 brings all the signals of both parts, including two separate processor buses, off of the chip, and the two can actually be used as separate processors.

Motorola has made several enhancements to this base design, however, so the whole is more than the sum of the parts. Both designs were reimplemented in a 0.65-micron CMOS process (from 0.8 micron), reducing their size and increasing the maximum clock rates. The new designs are fully static, so power consumption can easily be reduced by downshifting the clock. New on-chip PLLs can generate the necessary frequencies from a low-cost 32-kHz crystal.

Several features aim to reduce operating power. Separate PLLs allow either core to be slowed or shut down when not in use. The 68000 includes doze, standby, and stop modes for power management. The maximum power of the chip is 1 W using a 5-V supply and just 330 mW at 3.3 V. Using the power-management modes will reduce power consumption from these figures.

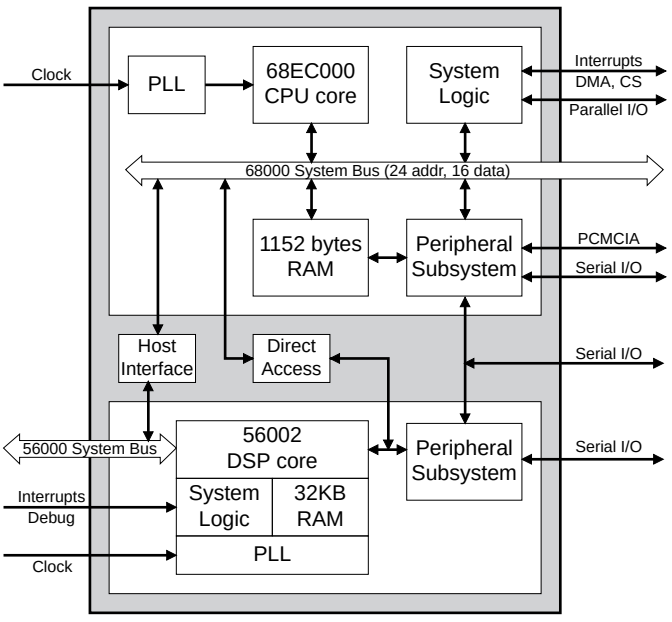

Figure 1. The 68356 combines 68000 CPU and 56002 DSP cores with extensive system logic and peripherals.

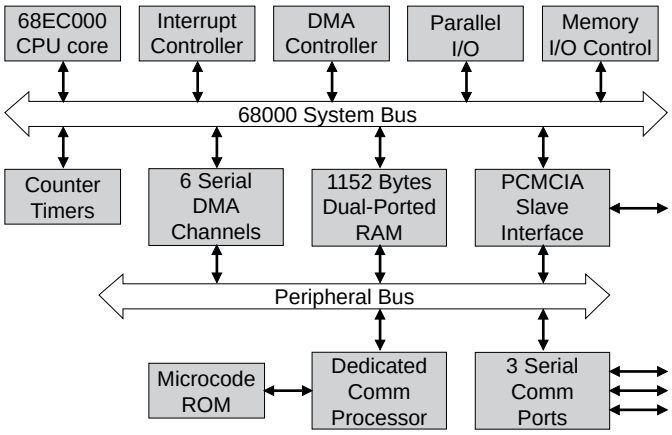

Figure 2. A detailed diagram of the 68000 portion of the chip shows the autonomous I/O processor that helps transfer data among the various serial channels.

Another new feature is the PCMCIA port, which is connected to the 68000 core. This is a slave-mode interface for use in a PCMCIA card; the 68356 requires an external controller to serve as a PCMCIA master. The 68356 is compatible with 8- or 16-bit PCMCIA interfaces up to version 2.1. The 68000 side of the chip also has new logic to emulate a 16550 UART. This logic provides complete hardware and software compatibility with this popular device, allowing the 68356 to function as a PC-compatible serial port.

The 56002 DSP core has been modified to include large on-chip memories for instructions and data (about 16K each). In addition to the normal synchronous serial port (SSI in Motorola terminology), the 68356 includes an asynchronous serial port (SCC) controlled by the 56002.

There are three ways for the 56002 core to communicate with the 68000 core. The 56002's new SCC port is connected internally to one of the SCC ports in the 68302 peripheral subsystem. This path provides a simple way to transfer data that has already been serialized. The 56002's normal 8-bit host interface is connected to the 68000 bus for traditional host/DSP communication. The 56002's 24-bit processor bus is also connected to the 68000 bus, allowing the DSP to easily read data from memory on that bus.

Extensive Communications Capabilities

As with most 68300 processors, the 68356 includes a set of system logic around a static 68000 core. This eliminates the need for most external glue logic. As Figure 2 shows, the 68000 portion of the 68356 has an interrupt controller, three timer/counters, a DMA controller, up to 36 parallel I/O signals, four chip selects, and control signals for standard DRAM, providing a glueless memory interface. Memory is connected to the 68000 system bus, which can be configured in either 8- or 16-bit mode.

The 68356 also includes the peripheral block from the 68302. This block features a set of devices organized around a 16-bit peripheral bus that is clocked at the speed of the CPU. The peripherals include three serial channels, one of which is connected to the 56002, as noted previously. The PCMCIA slave interface and the 16550 UART also connect to the peripheral bus.

As in the 68302, a microcoded communications processor (which Motorola calls a RISC CPU) provides protocol support for the three serial channels. This dedicated processor includes microcode for a variety of protocols: HDLC/SDLC, UART, BiSync, and transparent mode. The communications processor is capable of implementing any of these protocols independently on each of the three serial channels, relieving the 68000 CPU of all protocol overhead. The processor also has microcoded autobaud routines that can recognize the speed and format of an incoming serial data stream and configure the serial port accordingly.

The 68356 has a 1,152-byte RAM that connects the 68000 bus with the peripheral bus. This block of RAM is dual ported, allowing it to service accesses from both buses at once. A six-channel serial DMA controller also connects to both buses, controlling data transfers into and out of the dual-ported RAM. For example, a stream of data can be sent to a serial port by first transferring the data from main memory into the dual-ported RAM, then copying it to the serial port. Because both transfers can be performed by DMA, all the CPU need do is create the original data anywhere in main memory, set up the DMA transfers, and then move on to other processing.

Fast DSP Includes Plenty of Memory

The DSP is an enhanced version of the 56002, the most powerful member of Motorola's 56000 integer DSP family, which uses an unusual 24-bit architecture. This compromise between 16-bit and 32-bit designs delivers the resolution needed for high-quality audio processing at a lower cost than full 32-bit floating-point DSPs. (For modem applications, the 24-bit architecture is not required, since most calculations can be done to 16-bit resolution, but the extra bits in the 56000 architecture simplify some operations.) The 56002 is similar to the original 56001 but adds a double-precision multiply-accumulate (MAC) unit.

The 68356 DSP accepts a clock input of up to 60 MHz, but instructions are executed at one-half of the input-clock speed. Thus, the maximum instruction rate is 30 MHz (33-ns instruction cycle) at 5 V.

As Figure 3 shows, the 56002 core uses the three-bus architecture common to many DSPs: a program (instruction) bus and two separate data buses (X and Y). The X and Y buses feed operands into the MAC unit, allowing it to launch a new operation on every instruction cycle. The MAC unit contains a 24 × 24-bit multiplier

and a 56-bit accumulate register.

An ALU and a bit-manipulation unit perform simple integer and logical operations with single-cycle latency. The address-generation unit calculates up to three addresses per cycle, one for the instruction bus and one each for the X and Y data buses. The chip supports linear, modulo, and reverse-carry addressing. Modulo addressing can be used for circular buffers and lookup tables, while reverse-carry (bit-reversal) is useful in fast Fourier transforms (FFTs).

The program control unit (PCU) obtains and decodes 24-bit instructions and controls the execution units. A typical instruction can load two operands from on-chip memory and execute any arithmetic operation, including a MAC. The PCU implements zero-overhead looping to speed repetitive calculations. It contains a simple but fast interrupt controller with two standard interrupt inputs plus NMI.

The relatively small memories (less than 1K words) of the original 56002 core are greatly expanded in the 68356. The new program memory holds 5.25K instruction words (15.75 Kbytes) in SRAM along with boot code in ROM (64 words). The data memory contains 5.5K data words (16.5 Kbytes) of SRAM; it also has a 512-word ROM containing constants for sine and μ-law/A-law (compression) calculations. The dual-ported data memory can service requests from both the X and Y buses simultaneously.

Information can be loaded into this memory using the 56002's 24-bit external bus. For a low-cost implementation, however, the memory can be loaded from 8- or 16-bit memory on the 68000 system bus using the direct access mode. The combination of the large on-chip memories and direct access to the 68000 bus can eliminate the need for any memory on the 56002 bus.

The 56002 section of the chip contains a synchronous serial port, which is typically connected to the codec in a modem application, and a new asynchronous serial port. Because the latter is shared with one of the 68302's three serial channels, it is typically used to communicate with the 68000 CPU, although it can be used to access external devices if the 68302 is not using that port.

Motorola plans to offer a special version of the chip, the 68356M, that adds additional ROM space to the DSP program memory to hold the code needed for a V.34 28.8-kbps modem. This version would otherwise be identical to the standard part. By including this code, Motorola saves the system designer from adding an external ROM and also from having to develop or obtain V.34 code. Because the V.34 standard has not yet been finalized, the company does not have a schedule for this version.

Ball-Grid Array Reduces Cost

Allowing external access to all the signals of both the 68302 and 56002 processors gives the 68356 a high pin count: 357 pins. Traditionally, such a pin count would require a costly PGA package, as it is too large for a standard PQFP. Instead, Motorola has placed its new chip in a ball-grid array (BGA) package, a technology that the company developed internally but has now licensed to other vendors *(see **071203.PDF**)*. The 357-pin BGA package is less expensive than a PGA and smaller than a 132-pin PQFP. The 68356 is the first merchant-market microprocessor to use a BGA package, although Motorola has placed peripheral chips in BGAs.

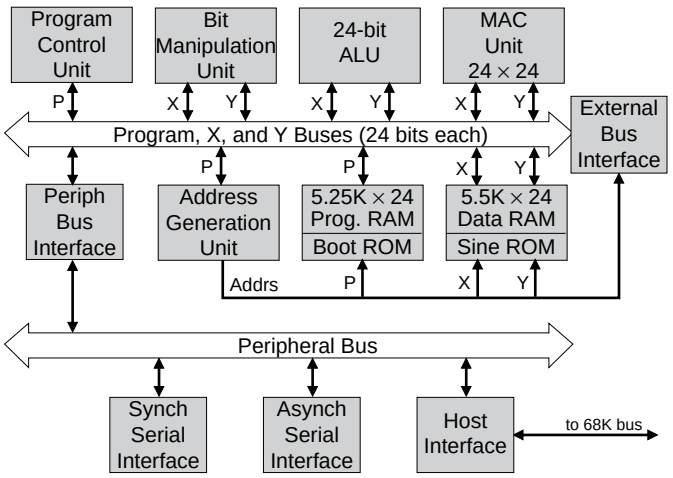

Figure 3. The 56002 portion of the chip contains large banks of program and data RAM connected directly to a fast multiply-accumulate (MAC) unit and other signal-processing logic.

Motorola has taped out the part but has not yet received first silicon of the new chip, and the company is not willing to divulge the die size of the part. The transistor count is 2.15 million; more than half of these are used for the 32K of SRAM on the chip. Based on this transistor count, the die size of the part should be fairly reasonable, about 100 mm^2 or a bit smaller.

An interesting question, which at this point must go unanswered, is how the manufacturing cost of the 68356 compares with the cost of building separate 68302 and 56002 dice. In general, the cost of building one large piece of silicon is greater than that of two small pieces. For relatively small chips, however, there are significant packaging and testing costs that are reduced by combining two chips into one. For this type of part, the manufacturing cost premium for a single larger chip is only a few dollars.

Another way to do the comparison is based on price. According to Motorola, combining the 10,000-unit prices of a 25-MHz 68302, a 60-MHz 56002, and 32K of external SRAM results in a price of about $70 for a discrete solution. Even this combination of parts would not include a PCMCIA interface and host bus interfaces, which might cost another few dollars each. The 68356, by comparison, is priced at $65 in the same quantity.

Price & Availability

Motorola expects to sample the 68356 in August, with volume production in the fourth quarter. Production pricing is set at $64.95 in quantities of 10,000 units. Pricing and availability for the 68356M is not yet set, pending finalization of the V.34 standard. The 68356 development kit—which includes a development board for an IBM PC or Sun 4, a logic-analyzer interface, and debugger software for both the 68K and DSP portions of the chip—will be available in 3Q94 at a price of $1,995 in unit quantities.

For more information, contact your local Motorola sales office or call Rex Kiang at 512.891.2429; fax 512.891.8807.

Thus, if a designer makes use of all features of the 68356, the new part would result in a smaller footprint and reduced power consumption as well as a cost savings of a few dollars. If the designer could get by with a different configuration—say, a slower CPU or less SRAM—the cost savings could easily disappear, but the 68356 would still offer power and integration advantages.

It is difficult to compare the 68356 to other vendors' products, as there are no products offering a similar feature set in a single chip. Many current applications combine the popular 68302 with a discrete DSP from Motorola or another vendor, such as TI, AT&T, or Analog Devices. One could replace the 68302 with an inexpensive RISC processor, such as an i960SA, that offers better CPU performance, but such a design would require several external parts to duplicate the system logic and peripheral set of the 68302, particularly the communications processor.

By integrating the DSP with the processor, Motorola is challenging other DSP manufacturers that do not have access to a CPU core. Designers who have been using non-Motorola DSPs must abandon their current DSP supplier to select the 68356. TI, AT&T, and other DSP makers may experience declining sales in those markets where the 68356 is most applicable.

Designed for High-Speed Modems

Motorola has made a good business from the 68300 line by creating highly integrated designs for specific applications. The 68356 is well suited for a specific target: PCMCIA cards for wired or wireless modems. These cards have very little real estate, and the 68356 puts the right feature set into a single package measuring one square inch. The power-reduction features are ideal for a battery-operated device. This market, while small today, is growing rapidly. Non-PCMCIA modems may also find the 68356 a useful way of integrating a number of discrete components in current designs.

Another area for the 68356 is in two-way pagers and other portable messaging devices. These products would not use the PCMCIA interface but could take advantage of the fast DSP for wireless communications. The 68000 CPU provides adequate performance for simple control functions in these devices, and the 68356's high degree of integration and low power consumption would allow for small devices with long battery life.

Designers may also take advantage of the 24-bit audio capability of the 56002 by using the 68356 as an autonomous sound processor. Although some systems can use the main CPU to control audio processing, that CPU may not be able to provide adequate response time when running a non-realtime operating system like Windows. By using the 68000 CPU to control the DSP, a system can ensure realtime response for audio processing without changing the software on the main CPU.

The 68356 plays into Motorola's strengths in the communications market, both as a component and a system provider. The new chip leverages the existing infrastructure of tools and software for the 68000 and 56000 product lines.

As with most other 68300 products, however, the 68356 is less suited to a broad range of applications and is not intended to be a general-purpose solution. In tuning the chip for a particular target, Motorola has included features that are not useful in other designs, such as the PCMCIA interface. Furthermore, the combination of the 68000 and 56002 is not appropriate for all applications. A PDA, for example, needs a faster CPU to go with the fast DSP, as well as PCMCIA master capabilities. An industrial controller, on the other hand, could get by with a less expensive DSP than the 56002.

For portable modem designers, the 68356 is a good solution, saving board space and power. Other designers who find the chip intriguing, but not quite suited for their particular application, may wish to talk to Motorola about its FlexCore program *(see **0807MSB.PDF**)*, which can generate a design tuned to any specific application—provided the volume exists to justify a custom design. Lower-volume applications may be stuck with discrete solutions unless they can latch on to a standard part in Motorola's burgeoning 68300 family.

With the 68356, Motorola pioneers a new level of integration, combining three different processors, memory, and peripherals on a single chip. The part takes advantage of Motorola's vast design library, which contains CPUs, DSPs, and the other components needed for this device. It also demonstrates again the company's ability to quickly and effectively integrate a variety of components. As the embedded market demands devices that incorporate nearly an entire system on a chip, Motorola is well positioned to deliver such products; other embedded vendors may find it more difficult to match Motorola's range of solutions. ♦

