Most Significant Bits

Alpha Sizzles, Thunder Rolls at Hot Chips

At the recent Hot Chips conference, Digital unveiled its next-generation Alpha processor, the 21164. Code-named EV-5, the CPU dispatches up to four instructions per cycle into dual integer units, an FP ALU, and an FP multiplier. It uses a seven-stage pipeline similar to the 21064's but with improved latencies for some operations. In addition to dual 8K instruction and data caches, the chip contains a large (96K) secondary cache that has an eight-cycle latency.

At its target frequency of 300 MHz, the 21164 will outperform all current processors, but it remains to be seen how it stacks up against next-generation offerings from other vendors. Digital did not reveal any price or availability information at the conference. (We will feature additional coverage of the 21164 in our next issue.) *(see **081201.PDF**)*.

Metaflow gave an overview of its Thunder CPU, a SPARC processor based on the never-shipped Lightning design (see MPR 9/19/90, p. 4). Like its predecessor, Thunder uses a dataflow model that allows instructions to execute out of order. It can issue four instructions per cycle into eight function units (three integer ALUs, two memory units, two FPUs, and one branch unit). The processor includes a cache controller and an MBus interface.

Using 0.8-micron CMOS, the Thunder design takes three chips, one less than Lightning, totalling six million transistors. At 50 MHz, the chip set is expected to reach 120 SPECint92. This version could ship by mid-1995. A 0.5-micron version, expected to hit 80 MHz, should quickly follow, pushing performance to 190 SPECint92. The current design is built by VLSI Technology and will be marketed by Hyundai.

National had planned to announce a new CPU architecture at the conference but withdrew at the last minute. It appears that the new processor has suffered a schedule slip. National still plans to describe its new chip at the Microprocessor Forum in October.

Digital Ships 275-MHz 21064A

Even as the company revealed its next-generation CPU, Digital has begun shipments of its 21064A, which was first announced last fall *(see **0714MSB.PDF**)*, about two months ahead of schedule. The new processor is now available in volume to system vendors at 233 and 275 MHz, priced at $875 and $1,192 in 1,000-unit quantities.

Digital also announced its first new workstations that take advantage of the 21064A. At the high end, the Model 900 uses a 275-MHz CPU, with a 2M external cache, to achieve 189 SPECint92 and 264 SPECfp92. The integer ratings are a bit better than expected but FP performance lags the original estimate of 290 SPECfp92. The company says that the higher estimate is for a server with a fast 4M cache, which should come closer to the original estimate. The Model 900, with a 21" monitor, 64M of memory and a 1G disk, lists for $43,373.

Digital also announced the Model 700, which contains a 225-MHz 21064A processor, also with 2M of external cache. This system, which lists for $27,698 in the same base configuration, is rated at 163 SPECint92 and 230 SPECfp92. The 233-MHz 21064A should achieve slightly higher ratings.

The company also reported SPECbase results *(see **0803MSB.PDF**)* for the new systems. Without extensive compiler tuning, the 21064A delivers a respectable 94% of its peak integer performance and 92% for FP.

VLSI, Intel Cancel Draco, PDA Agreement

Suffering from the chill in the PDA market, Intel and VLSI Technology announced that they have dissolved their partnership to build integrated microprocessors for the handheld computing market *(see **0610MSB.PDF**)*. The partnership was intended to combine Intel's 386 and 486 CPU cores with system logic from VLSI's portfolio, creating low-cost, low-power chip sets for PDAs. The first such product, the two-chip Polar, was announced with much fanfare last fall *(see **071302.PDF**)*. Compaq said that it would build a "mobile companion" based on the 386-class Polar chip set.

Since that announcement, the market for PDAs has developed more slowly than anticipated: neither the Casio/Tandy Zoomer nor Apple's Newton has made a big splash, and AT&T's Eo products have failed entirely (see next item). Compaq's PDA, originally planned for a midyear debut, has slipped to early 1995.

Compaq says that its schedule slip is market driven, although both core technologies for its device have also slipped. The Polar CPU, originally planned for 1Q94, is just now beginning to ship, and Microsoft's WinPad operating system has slipped to the end of the year. Compaq plans to forge ahead with its Polar-based device, and both VLSI and Intel expect to supply Polar to all current customers. Neither company plans to market Polar to new customers, however, seeing a lack of demand for 386-class performance in a handheld device.

The former partners had been developing the Draco chip set *(see **0709MSB.PDF**)*, based around a 486 CPU, to solve the performance problem. With the dissolution of the agreement, however, the nearly completed Draco design will be shelved. Intel plans to sell its 5% ownership of VLSI, which it acquired when the partnership was formed.

Neither company offered substantial comment on the reasoning behind the breakup, blaming it solely on

poor market demand. VLSI, however, remains quite committed to the PDA market through its ARM program (see below), so it may be Intel that broke off the relationship. But the CPU giant cannot completely ignore the developing handheld market and is rumored to be working on Intel-only solutions to be deployed when the market reaches a larger size. Perhaps the VLSI arrangement was a marriage of convenience to bridge the gap until Intel can market its own PDA processors.

AT&T Ends Last Chance for Hobbit

AT&T has shut down its Eo subsidiary, which had been struggling to develop a next-generation product after the failure of its initial Communicator. The new device, which was said to be closer to an enhanced cellular phone than a tablet computer, was the only remaining application using the Hobbit microprocessor. AT&T terminated all future Hobbit development efforts earlier this year *(see **0803MSB.PDF**)* but said that the product line could survive if Eo's smart phone was successful.

The demise of Hobbit illustrates the folly of basing a microprocessor strategy on a single operating system, for a single application, in a not-quite-emerging market. That ARM is more successful stems not so much from Newton's modestly greater success (relative to Eo) but from its use in a wide variety of applications.

Hobbit was once to be the heart of Newton, but Apple switched to ARM because of a variety of technical and business concerns. AT&T tried to get General Magic, in which it is an investor, to use Hobbit, but General Magic's engineers declined, citing cost and performance concerns. AT&T chose not to support Hobbit for other embedded applications because of the investment in tools and support that would have been required and because of a mistaken belief that its position would be strongest if it focused on a single key application area. Eo's demise also ends any prospects for the PenPoint operating system, which Eo had acquired.

Letter to the Editor

We were surprised and disappointed at a number of comments you made in your article on the Intel/HP alliance *(see **080801.PDF**)*. While we agree that the press announcement was important, we don't believe that there was enough substance to warrant many of your speculations.

The most disturbing statement was the supposition that "the PowerPC alliance would be the most distraught." Far from distraught, we are delighted that Intel has now joined the chorus of those saying that the x86 simply cannot keep pace. Of course, we expected that, at some point, Intel would have to offer its customers a migration strategy from the x86. And we expected that Intel would tell its customers that the transition path would be teflon-smooth. But we are elated that Intel has made these statements half a decade before they expect to have the product available. We expect that the products PowerPC will offer over the next 18 months will offer a far more compelling migration from x86 than Intel's promise of a blissful migration in the distant future.

Intel's vaporous "post-RISC" design is nothing more than the latest theme from the same marketing department that claimed both Pentium and the 486 to be RISC. Since actual parts aren't promised until nearly the end of the millennium and there is no evidence that the yet-unnamed architecture will actually be a superior design, we will simply ask customers whether they are willing to wait five years for promised better-than-x86 performance from Intel, or whether they prefer to buy something that offers better performance and far better price/performance right now.

The Intel/HP announcement is important, but there is a long gap between an announcement and the delivery of products. Intel has made dramatic announcements about futuristic processors before, only to have its partnerships quietly fade away years later.

—Michael Mace, Competitive Analysis Manager
—Apple Computer

VLSI Shows Two New ARMs

With a two-fisted announcement, VLSI Technology revealed an enhanced version of the ARM610 along with the ARM710, its first product based on the ARM7 core *(see **071503.PDF**)*. The 710 combines the ARM7 core with 8K of cache, a Newton-compatible MMU, and a bus interface. The 710 is faster than originally expected, reaching 40 MHz with a 5-V supply. At this speed, the chip delivers 34 Dhrystone MIPS.

Power dissipation, on the other hand, is slightly lower than anticipated, just 500 mW at full speed with a 50-pf load. The chip runs at 25 MHz with a 3.3-V supply, reducing power consumption to 125 mW. At this voltage, the 710 delivers slightly better performance than the original 20-MHz 610 at about one-quarter of the power.

The new 610 uses the same 0.8-micron process as the 710 to increase the clock speed to 33 MHz at 5 V, a 65% improvement over the original 610, with the same 500-mW power consumption. The chip is function- and pin-compatible with the original 1.0-micron version.

Both new processors are currently sampling, with production slated for October. The 33-MHz 610 is priced at $17 in quantities of 10,000. In the same quantities, the 40-MHz 710 sells for $20. Apple will probably use one or both of the new ARMs to upgrade the performance and extend the battery life of its Newton line, which continues to sell reasonably well into vertical markets.

Separately, ARM announced that its architecture has been adopted by Asahi, a Japanese vendor of telecommunications chips and other ICs. The company is a

leading supplier of mixed-signal chips, which combine analog and digital components. Advanced RISC Machines (ARM) hopes that this speciality will allow Asahi to differentiate its ARM-based products from those of other ARM licensees: Cirrus, GEC Plessey, Samsung, Sharp, TI, and VLSI Technology. The agreement gives Asahi access to the ARM7 core.

ARM chips have proved popular for consumer electronics due to their low cost and power consumption. Equally important, however, has been the company's broad licensing strategy, which allows for multiple sources, whereas competing products (such as Motorola's 683xx and NEC's V800) have only a single source. Furthermore, ARM has selected partners that have a range of technical capabilities. One weakness is the lack of a high-end offering; architectures such as MIPS and PowerPC offer a broader range of performance points.

IBM Deploys MPEG-2 Decoder

Continuing its aggressive move into the merchant chip market, IBM Microelectronics has announced a single-chip MPEG-2 decoder. This is IBM's first foray into the video compression market, although the company has been marketing a lossless compression chip for disk drives and similar applications. Instead of starting with a simpler MPEG-1 design, the company has jumped into the high end of the video market, aiming at set-top boxes and other broadcast video applications.

Although AT&T has beaten IBM to market with an MPEG-2 decoder chip *(see **0801MSB.PDF**)*, IBM's device is the first to implement the complete MPEG-2 Main Profile, including bidirectional (B) frames. IBM's decoder also implements advanced features such as error concealment and flexible 8- or 16-bit YUV and YCrCb output. The chip can also handle MPEG-1 video, expanding it to full CCIR resolution if required. The device uses an internal RISC processor (that is not based on PowerPC) to allow more flexibility than hard-wired solutions.

The decoder takes advantage of IBM's 0.65-micron CMOS-5L process (also used for the PowerPC 603) to place about one million transistors on a compact die measuring 66 mm^2. The chip uses a 208-pin CQFP and, at 3.3 V, dissipates about 1 W. It requires 2M of external DRAM for MPEG-2 operation.

The decoder is currently sampling; IBM expects it to reach volume production in 4Q94. The 1,000-piece price is $98, but the MPR Cost Model *(see **071004.PDF**)* estimates the manufacturing cost at $32, indicating that high-volume customers could receive a much lower price. These lower prices are required to put the chip—along with a CPU, memory, and analog interfaces—into a $300 set-top box, the nirvana of digital convergence.

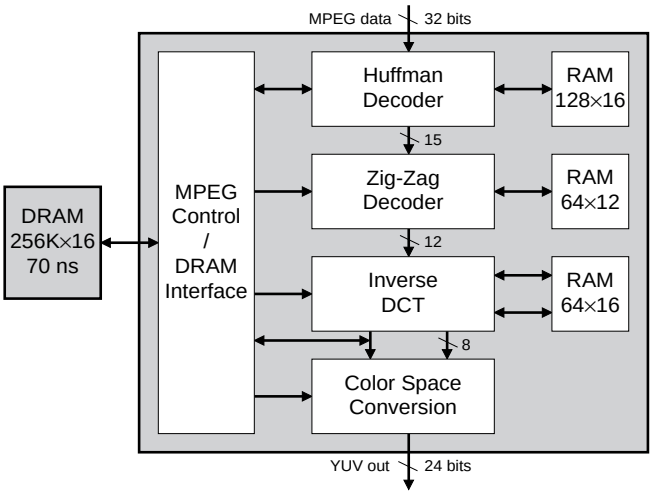
Cirrus Licenses MPEG Core from CompCore

Giving startup CompCore Multimedia a big boost, Cirrus Logic has licensed an MPEG-1 decoder engine from the tiny Sunnyvale (Calif.) company. CompCore has a unique approach to the MPEG market: instead of selling a decoder chip, it is marketing its technology as a core logic design that can be combined with other graphics or video circuitry on a single chip. Implemented in 0.6-micron CMOS, the MPEG decoder (including 480 bytes of scratch RAM) uses only 16 mm^2, allowing it to be easily added to an existing design.

CompCore uses a number of techniques that greatly reduce the size of its decoder, including a unique method of parsing the MPEG data stream. The design also uses a proprietary algorithm that performs a mathematical transformation on data encoded using DCT (discrete cosine transform) compression. This transformation simplifies the operations needed to calculate the inverse DCT function, reducing the amount of logic required. The figure below shows the basic CompCore design, which uses 512K of external memory.

Cirrus plans to combine the MPEG core with its own graphics, video, and audio circuits to develop low-cost PC multimedia controllers. The company did not offer any details on the availability of these products, but they will probably not begin shipping before next year.

For very low cost systems, such as set-top boxes, the video decoder may reside on the CPU chip. CompCore is pursuing other licensees, including Zilog and 3DO. The startup is working to extend its design for MPEG-2 and is also developing an MPEG audio decoder. By offering its design as a licensable core, the company is taking advantage of a trend *(see **081001.PDF**)* toward customers combining circuit designs from various sources to create custom solutions. This strategy allows CompCore, a five-person company, to compete successfully against much larger vendors like IBM (see previous item). ♦



CompCore's MPEG-1 video decoder can be implemented with just 7,500 gates, 1,200 bits of registers, and 480 bytes of RAM.

