Most Significant Bits

3DO Chooses PowerPC for Next Generation

Seeking to boost its performance beyond that offered by the ARM processor family, game-maker 3DO is developing a PowerPC-based design that will also include new graphics-acceleration hardware, providing a dramatic performance boost for future games. Although 3DO's sales have been lackluster so far, this win is significant for the PowerPC camp, as it shows that the architecture is moving into a broader range of applications. It also highlights a weakness of the ARM architecture that could eventually compromise its position as the heart of Newton as well: its lack of a high-performance implementation, either now or in the near future.

Although the announcement has been positioned as a joint IBM/Motorola design win, sources indicate that 3DO's relationship has been primarily with IBM, and that 3DO was attracted to IBM in large part because of its high-density ASIC technology. (Contrary to press reports, the 3DO design has nothing to do with Motorola's FlexCore custom processor program.) After starting at IBM, the project moved to Somerset, and both IBM and Motorola will build the processor. The chip is expected to find applications beyond 3DO's system, and IBM and Motorola are likely to offer it on the merchant market.

Seeking to match Nintendo's 64-bit claims for its future R4000-based game, 3DO's press release spuriously touts the new system's use of a "64-bit" PowerPC processor. This claim prompted speculation that the design would use the 620 core, the only near-term 64-bit implementation. The 620 would be prohibitively expensive, however; informed sources indicate that the processor uses a new 32-bit PowerPC core. The chip, like other PowerPC processors, uses a 64-bit bus but not the same bus as the 60x devices.

Unlike most other embedded processors, fast single-precision floating-point performance is a high priority for the 3DO processor because of its value in performing 3-D transformations. It is not clear whether graphics and other functions have been integrated on the processor or if these functions are in a separate ASIC.

The first 3DO product to use a PowerPC processor will be an upgrade cartridge, called M2 and due by Christmas 1995, for the company's existing Multiplayer game machines. A new system with a built-in PowerPC processor is due to follow, probably in 1996. Ironically, sources indicate that the use of PowerPC won't mean lost sales for ARM, at least in the next couple of years: the PowerPC system will retain the ARM processor to provide compatibility with first-generation 3DO games. 3DO developed a software emulator for ARM that runs on the PowerPC chip, but the ARM processor actually costs less than the ROM space needed to hold the emulator.

This transition will put 3DO in a much better position to compete with next-generation game systems from Nintendo, Sega, and Sony *(see **080902.PDF**)*. As in any architecture transition, though, there are dangers. Game developers may be hesitant to target the soon-to-be-obsolete ARM version of the platform, but there won't be a meaningful installed base of the PowerPC version until sometime in 1996. And once developers make the switch to creating PowerPC games, they won't be able to sell the new games to customers that haven't purchased the upgrade module. 3DO plans to price the upgrade aggressively and believes that the performance increase will be so compelling that the vast majority of system owners will upgrade by sometime in 1996.

SuperSparc-2, UltraSparc Delayed

Sun and foundry Texas Instruments have encountered delays on their SuperSparc-2 (SS-2) project, representing the first break from Sun's "guaranteed" SPARC roadmap *(see **070404.PDF**)*. The company had originally asserted that the follow-on to SuperSparc would begin volume shipments in 3Q94, but the part has not yet begun to sample. Sources indicate that Sun is still debugging initial prototypes and that system shipments are not likely before the end of this year. SS-2 is now expected to hit 90 MHz, boosting SPARC performance to about 125 SPECint92.

The more complex UltraSparc is also behind schedule. Sun's roadmap shows the next-generation processor sampling this quarter and reaching system shipments shortly after the end of the year. Yet sources indicate that the device has not yet achieved first silicon, making system shipments unlikely before 3Q95, a six-month slip. The current expectation is that UltraSparc will miss its 275-SPECint92 goal by 10%, although either compiler enhancements or frequency increases may still save the day.

In the meantime, Sun's fastest processor is the 60-MHz SuperSparc, a chip that is outperformed by Pentium as well as by several RISC processors. To improve its position, Sun may turn to Ross Technology's HyperSparc processor, which today delivers about 20% more performance than SuperSparc. SMCC, Sun's system arm, continues to evaluate the Ross chip and, as SS-2 slips out, may commit for the first time to shipping systems using a SPARC processor that was not designed by Sun.

The delays show that Sun, while improving, continues to be overaggressive in its claims for future processors. The company did well in delivering MicroSparc-2 on time and has even seen some upside on the clock speed of that part. The more complicated SS-2 and UltraSparc, however, have taken longer to design than Sun intended

and are lagging their performance goals. So far, these problems are similar to those seen in other high-end processors, but further slips will jeopardize UltraSparc's goal of reducing the SPARC performance gap.

Analog Sinks SHARC Price

Moving its SHARC chip downstream, Analog Devices has introduced a low-cost version of the DSP, dubbed the ADSP-21062. The new chip is identical to the high-performance 21060 *(see **071602.PDF**)* except that it contains just 2 Mbits of on-chip memory instead of 4 Mbits. Both chips have a peak performance of 40 native MIPS and 80 MFLOPS.

Reducing the size of the large on-chip memory array cuts array the die area of the chip from an enormous 275 mm^2 to 172 mm^2. The price of the 21062, in 1,000-unit volumes, is $196 for 33-MHz parts and $249 for the 40-MHz version. These prices are about one-third less than the prices of the high-end 21060 DSP. Even at the lower price, however, the SHARC design is far too expensive for most DSP applications, appealing only for products such as cellular base stations and color fax/printers that require maximum performance and can afford to pay top dollar.

AMD Moves 486DX2 to 80 MHz

Matching Cyrix's top announced speed, AMD has announced immediate availability of 80-MHz 486DX2 processors. These processors are identical to AMD's original DX2 chips *(see **070601.PDF**)* and offer a convenient upgrade for systems using the company's 40-MHz 486DX. Following its traditional pricing strategy, AMD is offering the 80-MHz version at the same rate as its 66-MHz part: $266 in 1,000-piece volumes. This price is nearly the same as Intel's price for its 66-MHz 486DX2.

Cyrix had earlier announced its own 80-MHz 486 *(see **0808MSB.PDF**)*, using IBM's 0.7-micron process, but the company has not yet begun to ship 80-MHz parts. AMD has managed to squeeze 80-MHz operation out of its own 0.7-micron process; the new parts use the same process and same die as the 66-MHz version. Note that Cyrix's fast parts operate at 3.3 V, while AMD's DX2 chips run at 5 V.

AMD is pushing forward on its next-generation 486 parts, which will use a 0.5-micron process to increase the clock speed to 100 MHz or possibly 120 MHz. These parts may include some features distinct from the DX2 chips, such as clock tripling and a larger, write-back cache. AMD expects to announce these parts soon and ship them by the end of the year.

Cyrix, Lone Star Dispute Incompatibilities

Lone Star Evaluation Labs (LSEL) has published a report detailing several inconsistencies between the 486DX parts from Cyrix and Intel. LSEL, led by Ed Curry, had earlier found a bug in the Cyrix part that caused it to generate incorrect floating-point results in some obscure situations *(see **080703.PDF**)*; this bug was fixed in a later revision of the Cyrix CPU.

The new report describes several other inconsistencies, none of which affect typical Windows code. These differences were found by running Intel, AMD, and Cyrix 486 chips through a suite of 20,000 tests that are hand-coded to exercise the processors. LSEL found no compatibility problems with the AMD chip, which uses the same logical design as Intel's 486 processors.

One inconsistency involves differences between the Cyrix and Intel processors when calculating tangents. The two processors always agree on the first 11 (decimal) digits of the result, but they occasionally differ in the last few digits for input values near $\pi/2$.

Cyrix explains that its 486DX, like the company's earlier math chips, uses a polynomial approximation for the tangent function, while Intel uses the older CORDIC algorithm. The polynomial method is more accurate and also faster but does generate slightly different results. Near $\pi/2$, the slope of the tangent function approaches infinity, increasing the magnitude of the differences.

In other situations, the Cyrix chip sometimes generates the floating-point result NaN (not a number) when the Intel processor calculates a response of zero. NaN is an unusual result typically caused by dividing by zero or taking the square root of a negative number. The code in question performs a series of floating-point calculations, including square root, but no tangents.

Oddly, the behavior of the Cyrix processor can be changed by altering the memory addresses of the variables without changing the code itself. (LSEL does this by inserting dummy variables into the C code.) Depending on the memory addresses, some calculations correctly return zero while others return NaN. This problem occurs only under Windows NT, a 32-bit operating system. Regardless of the addresses of the variables, the Intel processor always executes the code correctly.

LSEL has not been able to reduce this problem to the failing instruction and refuses to release the code to Cyrix for analysis. Without the code, Cyrix cannot determine if there is a bug in its processor. The results could indicate a problem in which the FPU generates incorrect NaN values; the address variability could indicate a stack or memory management problem.

From the Mailbox

Your piece on Gary Kildall was by far the best analysis of what Gary really contributed that I have seen.

—Gordon Eubanks, President, Symantec

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On the other hand, the NaN could be legitimately created if a series of calculations results in a value of zero on the Intel chip but generates an extremely small negative value on the Cyrix processor. The square root of these two results would be zero for Intel but NaN for Cyrix.

LSEL believes that it should be compensated for the work it has done before releasing the code to Cyrix. The CPU vendor feels that it shouldn't have to pay to look at an issue that may not even be a bug. Given this impasse, it is impossible for a third party to determine whether any of the incompatible results detected by LSEL actually represents a design problem in the Cyrix 486.

The circumstances indicate, however, that users running typical Windows applications should not see any of these problems. The inconsistencies appear only when doing very accurate floating-point calculations, or with 32-bit operating systems like Windows NT. Whether these inconsistencies represent a problem for any users at all is a question that can be resolved only if Cyrix and LSEL settle their differences.

The 26-page report on these inconsistencies sells for $30. For more information, contact LSEL at 512.746.2251 or fax 512.746.2187.

Via Intros First SLIC Chip Set

Becoming the first chip-set vendor to back Cyrix's rival MP standard, Via Technologies (Fremont, Calif.) has introduced a system-logic chip set, named Apollo, that supports the SLIC multiprocessor architecture. The Cyrix-designed SLIC *(see **0808ED.PDF**)* is intended as a more open alternative to Intel's APIC-based approach for dual-processor Pentium-class systems.

Ironically, the only available processors that are compatible with the Apollo chip set are Intel's Pentium processors. Apollo does not include Intel's I/O APIC, which is required to implement Intel's multiprocessor scheme. The chip set will support Cyrix's M1 and AMD's K5, however, when those CPUs become available.

Software support for the dual-processor configuration is expected to emerge later this year. Cyrix is developing a HAL (Windows NT hardware abstraction layer), which Microsoft is expected to include (along with one to support Intel's APIC design) in a future NT release.

The Apollo chip set consists of a 208-pin system controller, two 100-pin data buffers, and an optional 160-pin VL-to-PCI bridge. Without the bridge chip, the chip set is essentially a VL-Bus design suited for notebook systems. Via claims that its superior buffer design gives Apollo 10% better performance than competitive PCI chip sets.

Apollo supports up to 512M of DRAM and an L2 cache of 256K to 2M, using either synchronous or standard SRAMs. Via also offers a 100-pin Integrated X-Bus Peripherals Controller, which includes a clock generator, real-time clock, and keyboard controller. Apollo is available now, with pricing in OEM quantities starting at $28 for the 5-V version. A low-voltage version, compatible with 3.3-V Pentium processors, is also available.

According to Cyrix, more than a dozen chip set vendors have licensed the SLIC architecture. In addition to Via, Opti is committed to supporting SLIC in its forthcoming 64-bit chip set. Other x86 vendors, such as AMD and IBM Microelectronics, have endorsed SLIC over Intel's proprietary APIC standard *(see **080301.PDF**)*, as the Cyrix proposal requires no changes to the processors themselves. Motorola and IBM also have endorsed SLIC for PowerPC processors, although neither company would commit to delivering a chip set that implements the MP standard.

LSI Adds Rambus, PCI to ASIC Library

Expanding its CoreWare offerings, LSI Logic has licensed the Rambus interface. This license allows LSI customers to create their own ASICs that contain LSI's R3000 processor core and connect directly to Rambus DRAMs (RDRAMs). Several memory vendors are shipping RDRAMs *(see **070304.PDF**)*, which use a 500-Mbyte/s bus to transfer data to the host. LSI will offer the Rambus interface in 0.5-micron CMOS starting in 4Q94.

The company has also developed a PCI interface called PCI-32 FlexCore (not to be confused with Motorola's FlexCore program). This module allows ASIC designers to add an off-the-shelf PCI interface to their chips while configuring it to meet specific needs. The design has several selectable features that can be used to implement a variety of subsets of the full PCI specification, allowing the designer to trade off performance against die area. This design is now available in 0.6-micron CMOS and carries a $40,000 NRE charge.

LSI's two-year-old CoreWare program *(see **0603MSB.PDF**)* continues to expand, allowing customers to design highly integrated processor ASICs. Rambus and PCI are emerging high-bandwidth interfaces that are replacing proprietary approaches; these announcements let LSI and its customers take advantage of this trend.

Errata: Thunder Plans

Due to our own error, we incorrectly reported the marketing plans for Metaflow's Thunder processor *(see **0811MSB.PDF**)*. Although Metaflow is using a 0.8-micron version of the processor in development, the company does not plan to market this version; the first parts to ship will use a 0.5-micron process. Metaflow expects to ship these parts in early 1995. Hyundai, while providing financial backing for the Thunder project, will not market the processor chips except in its SPARC workstations. Metaflow will handle all processor chip sales. ♦

