NEC Launches Second V-Series Core

V850 Core Offers 60% More MIPS per MHz Than V810

by Linley Gwennap

Continuing to expand its V800 family of processors, NEC has announced a second-generation CPU core, the V850, that potentially offers much better performance than the original V810 core. Although the initial version is available only at 25 MHz, the V850 core delivers 29 Dhrystone MIPS, nearly the speed of the 50-MHz version of the V810. NEC plans to push the V850 core to 33 MHz and beyond. The new core also improves on the price/performance and power/performance ratios of the V810. The company has not yet introduced the new parts outside Japan.

The first chip using the new core, the V851, is scheduled to sample by the end of this year. As Table 1 shows, the V851 includes the new core, 32K of ROM, 1K of RAM, a PLL, and some basic peripherals. This peripheral set is not as generous as that of the V820, but it exceeds that of the basic V810. The new chip uses a 16-bit data bus similar to that of the V805; the data is multiplexed with 24 bits of address. It includes a new PLL that offers up to 5× clock multiplication.

NEC is quoting an aggressive price for the V851: ¥1,900 (about $19) in large volumes (100,000 units) for the mask-ROM version. Developers may use a PROM version that costs ¥4,000 in sample quantities or an EPROM version at ¥20,000. NEC expects the PROM versions to be available in December, with the production (ROM) version ready around mid-1995.

The V850 core gains its performance advantage from incorporating data memory on chip; the V810 core uses only slower, off-chip memory for data. Performance is also improved by a new multiplier that can perform a $16 \times 16 \rightarrow 32$-bit multiply in a single cycle (best case).

	V851	V820	V810	V805
Max Clock Speed	25 MHz	25 MHz	25 MHz	25 MHz
Dhrystone MIPS	29 MIPS	18 MIPS	18 MIPS	18 MIPS
Bus Width	16 bits	32 bits	32 bits	16 bits
Math On Chip	Int. Mult.	FPU	FPU	FPU
ROM On Chip	32K	none	none	none
RAM On Chip	1K RAM	1K cache	1K cache	1K cache
DMA, DRAM Control	none	yes	none	none
PLL, Timers	yes	yes	none	none
Serial I/O	2 ports	2 ports	none	none
Parallel I/O	67 bits	none	none	none
Est. Mfg. Cost	$8	$27	$9	$8
List Price (100,000s)	$19	$80	$20	$18

Table 1. NEC's V-series now consists of four members. The V851 is the first to use the high-performance V850 core.

The V850 core also includes new STOP and IDLE instructions that enable flexible power-saving modes.

Using Dhrystone 1.1, NEC rates the V851 at 29 MIPS when running at its maximum speed of 25 MHz. Power usage at this speed is only 250 mW (typical). The chip offers a good interrupt-response time of 11 cycles (0.44 µs at 25 MHz). The V851 will operate using supply voltages as low as 2 V. As Table 2 shows, it will deliver more than 300 MIPS/watt at this voltage.

The V851 design uses about 440,000 transistors, including the on-chip memory. Like other V800 chips, it is built in a 0.8-micron two-layer-metal CMOS process to reduce wafer cost. The ROM version will have a die area of about 42 mm^2 and use a 100-pin thin PQFP package with a 0.5-mm pin pitch. According to the MPR Cost Model *(see **081203.PDF**)*, the V851 will cost about $8 to build, about the same as the slower V810.

The V851 is just the first in a line of products using the V850 core. NEC plans to offer a ROM-less version to decrease the entry-level cost and a 33-MHz version to increase performance. Other planned versions will include more peripherals, as in the V820, and some will have flash memory on board instead of ROM. The company will also offer the V850 core as part of its ASIC library.

The outstanding MIPS/watt rating of the V851 suits it for any portable device that requires a significant level of performance, such as portable telephones, game machines, and possibly even PDAs. Even for line-powered devices, the price/performance of the V850 makes it attractive, and many consumer devices require low heat dissipation. The V810 already has a design win in Nintendo's CD-ROM game machine.

The V851's price is about the same as that of the ARM710, and the NEC chip includes more peripherals than the ARM processor, although the ARM is slightly faster based on Dhrystone. The V851 promises to deliver more performance than Hitachi's SH7604 with lower power and at a lower cost. In the intensifying competition for high-performance, low-power consumer devices, the V851 should more than hold its own. ♦

	5 V	3 V	2 V
Max Clock Speed	25 MHz	16 MHz	13.5 MHz
Dhrystone MIPS	29 MIPS	18.5 MIPS	15.5 MIPS
Power at Max Clock (typ)	250 mW	100 mW	50 mW
MIPS per watt	116 M/W	185 M/W	310 M/W
Temperature Range	-40–85°C	-40–85°C	-10–70°C

Table 2. The V851 can operate with supply voltages down to 2 V. The lower voltage reduces the performance and temperature range of the CPU but improves the MIPS/watt rating.

