ARM Reaches into Set-Top Boxes

Acorn, VLSI Produce Single-Chip Multimedia Controller

by James L. Turley

Acorn Computer Group, VLSI Technology, and ARM have teamed to build a highly specialized chip aimed squarely at creating the lowest-cost set-top box controller yet available. The new device merges an ARM7 CPU core and cache with existing audio and video control logic to produce a one-chip solution for multimedia applications.

Announced at last month's Microprocessor Forum, the new ARM7500 integrated multimedia processor is the most highly integrated ARM device yet made public. ARM's Mike Muller pointed out that the chip was created specifically for one customer, although VLSI may decide to offer it commercially to other video service developers or as a multimedia engine.

The ARM7500 was developed for Online Media, a U.K. subsidiary of Acorn Computer Group, the company that spun off Advanced RISC Machines (ARM) in 1989. Acorn, which is itself 80% owned by Olivetti, has been carrying out video-on-demand trials in Cambridge, England since August 1994 in association with Bell Northern Research. Those trials use an earlier generation of the set-top logic that the ARM7500 is designed to replace.

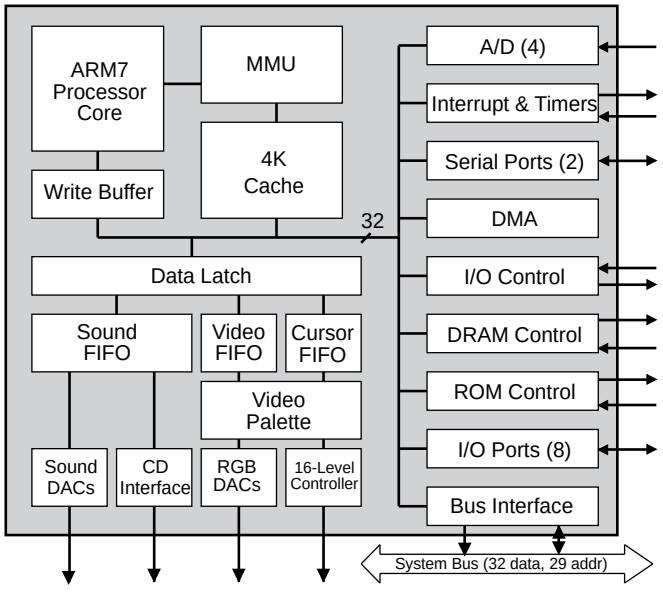


Figure 1. The ARM7500 integrates functions previously in separate devices in Acorn's set-top box. The processor block is essentially an ARM710 with a smaller cache. The audio and video blocks are taken from existing Acorn designs.

New ARM7 Implementation Used

The new multifunction processor combines into one chip most of the functions that were previously housed in several separate devices. The original box used a stand-alone ARM610 processor plus separate audio, video, and memory control chips. The 7500 integrates all these functions into one 240-pin PQFP.

In Online Media's system, the 7500 still needs external RAM and ROM, as well as cable and telephone line interfaces, a UHF tuner, and an intelligent ATM interface chip that itself contains another ARM core.

At its heart, the 7500 contains a new ARM processor. The new design features a 32-bit ARM7 core *(see **071503.PDF**)*, a memory-management unit, and a 4K unified instruction and data cache. The cache is four-way set associative and operates on a write-through basis. An eight-word write buffer isolates the processor from external delays during programmed store operations.

In the case of the 7500, the MMU and write buffer do not connect directly to external memory and I/O but to an internal 32-bit bus running throughout the device. The 7500's internal bus connects the CPU core to the integrated video, audio, memory, and peripheral control blocks, as illustrated in Figure 1. Ultimately, the internal bus is buffered and made available on external pins for connection to main memory and I/O devices.

Audio and Video Functions on Chip

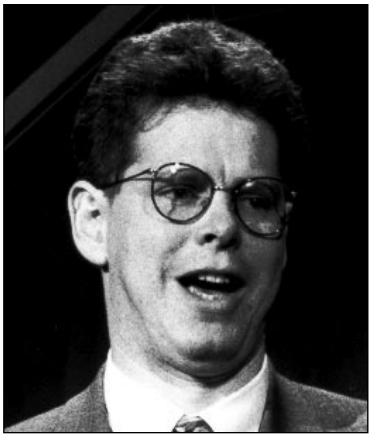
The peripheral blocks integrated in the 7500 were external devices in Online Media's previous box. The control logic used in that product was functionally identical to the 7500, except for an ARM610 processor in place of the 7500's ARM7-derived CPU. The video-control block was a separate VIDC20 device, while the I/O and memory were controlled by an IOMD chip. Both devices are still available from GEC Plessey, another ARM licensee.

The audio/video block connects three data FIFOs to the 7500's internal bus through a data latch. The FIFOs isolate the real-time requirements of the audio and video logic from the latencies involved in transferring data from external memory over a bus that must be shared by all devices on the chip. From the FIFO, audio data flows directly to an 8-bit audio DAC driving an external amplifier or speaker. In place of the analog audio channel, the 7500 also has a programmable option to provide a serial bit stream to drive external DACs for higher-quality sound.

Three 8-bit video DACs provide 256-color RGB output from a palette of 16 million colors. Pixel depth is programmable from 1 to 32 bits per pixel, in powers of two. Because there is no video memory on the chip, all pixel data must come from an external memory array. A 16-level grayscaler sits in parallel with the RGB DACs, providing the option to directly drive an LCD display instead of a color display.

Transferring all the data to the video and audio units is the task of the on-chip DMA controller. This unit has three channels, with each channel hardwired to feed either the audio, video, or cursor FIFO. The DMA has been tailored to run with little CPU intervention. The dedicated video channel, for example, can run in an infinite loop, refilling the video FIFO from the same block of memory with no CPU overhead. The ARM processor can even be stopped while the DMA maintains the display.

Internal address decoding with multiple programmable chip-select pins allows up to four independent banks of DRAM. Each bank can be either 16 or 32 bits wide, allowing wide banks for, say, video RAM and main memory and narrower 16-bit banks for small nonvolatile storage. An additional decode pin is dedicated to ROM selection, with programmable timing for two separate banks. The 7500 can optionally read from 16-bit ROMs, shifting address bits by one accordingly, for easier design.



MICHAEL MUSTACCHI

ARM's Mike Muller presenting the 7500 set-top box controller at the Microprocessor Forum.

To manage external memory, the 7500 includes DRAM control logic, with address multiplexing and enough current to drive RAS, CAS, and write-enable signals directly. Refresh cycles are generated automatically, with either CAS-before-RAS or self-refresh frequency programmable. Depending on the system loading, DRAM data can be gated directly onto the 7500's data bus with no additional transceivers.

Also included in the peripheral block is the basic control logic to drive commercial PCMCIA support chips, including execute-in-place (XIP) support. Four 16-bit A/D converters, two asynchronous serial ports, and eight general-purpose open-collector I/O pins round out the peripheral block.

Independent Clocking Supported

The 7500 allows the system designer to supply up to four separate clock inputs to the device. At least one is required, to pace the CPU, and by default, all other modules will operate from that source. As an alternative, the memory-control logic can be driven by a different clock input, making it easier to synchronize the memory bus with external peripherals or memory devices. Separate I/O subsystem and video clocks are also available.

Separating the CPU clock from the rest of the device makes it possible to vary processing speed while keeping other blocks synchronized with their external interfaces. Keeping the memory interface logic running at a fixed speed might be required to guarantee minimum DRAM refresh times.

The fully static CPU can operate to 33 MHz. When in idle mode, the CPU consumes almost no power, although other parts of the 7500 continue to work (assuming their clock sources are still active). The most power-hungry portion of the chip is the set of RGB video DACs; maximum power dissipation drops from 1.0 W to 0.5 W if the color DACs are not used. The CPU leaves idle mode and restarts on an active interrupt.

The 7500 will be produced at VLSI's San Antonio (Texas) fab, using the company's 0.6-micron two-layer-metal process. The die size is about 70 mm^2. Of that area, approximately 30% is the ARM processor itself, including its 4K of cache and its MMU. The MPR Cost Model yields an estimated manufacturing cost of $25 for the 7500. Commercial pricing is not available, as the device is currently produced only for Online Media's internal use in its set-top boxes. VLSI has turned out working samples, and limited production is scheduled to begin 1Q95.

Aimed at the Home

The television set-top box market—whatever that turns out to be—has captured many vendors' imaginations in the past several months. IDT, for one, has tailored its R4650 MIPS processor *(see **081504.PDF**)* for video capabilities. Where IDT's chip is more general-purpose in nature, the 7500 leaves no doubt what it is intended to do. The performance of the two devices is radically different—the 7500's estimated 30 Dhrystone MIPS is no match for R4650's 150 or more. Evidently ARM (or at least, Online Media) does not believe that processing power is the way to muscle into the set-top box market. ARM has loosed an arrow directly at the bulls-eye, while IDT is content to aim a big gun in the general direction of the target.

VLSI has its own plans for penetrating the emerging set-top market and might play no larger role in the life of the 7500 than serving as a fab for Online Media. On the other hand, the contract between the two companies allows VLSI to market the 7500 as a stand-alone commercial part, if VLSI so wishes.

In the consumer electronics market, part of the secret to success is keeping costs down and volume up. Custom hardware and a cheap, flexible CPU are vital ingredients. By that measure, the 7500 is right on track. ♦

