Literature Watch

ASICs

Toshiba samples 0.4-µm ASICs and gives projected specs for 0.15 µm. Production is scheduled for 1Q95 for a family of 0.4-µm ASICs by Toshiba, and projected specifications have been made for a 0.15-µm family for the end of the decade. *Computer Design,* 10/94, p. A4, 1 pg.

ASIC design methodologies change to keep up with deep-submicron geometries. As ASIC design goes deeper into the submicron realm, the need for parallel logic design and chip layout becomes more important to accurately predict timing. *Computer Design,* 10/94, p. A16, 5 pp.

Buses

VME and Multibus competitors agree on support for PCI extensions. Competitors agree to support the PCI bus as a local bus for VME and Multibus. Stephan Ohr, *Computer Design,* 10/94, p. 28, 3 pp.

Development Tools

DSP tools: navigating the hardware/software interface. DSP development tools are available to ease complex design and debug tasks. Ray Weiss, *Computer Design,* 10/94, p. 69, 11 pp.

Harness the power of VHDL for PLD design. A primer on designing PLDs with VHDL. Al Graf, Cypress Semiconductor; *Electronic Design,* 10/94, p. 108, 10 pp.

Leak detector shoot-out. Memory leak detectors Purify, Sentinel, and Insight are compared. James C. Armstrong, Jr., *Advanced Systems,* 10/94, p. 56, 4 pp.

Debugging with a nonintrusive monitor. A real-time nonintrusive (RTNI) monitor catches problems in embedded systems that occur only when software timing is undisturbed. Ralph Barrera, ITCN; *Electronic Design,* 10/3/94, p. ES-32, 2 pp.

Miscellaneous

ECL circuits show renewed promise thanks to active pull-down designs. Recent designs of fast ECL circuits employing several types of active pull-down (APD) offer hope of increased frequency with lower power. Cheryl Ajluni, *Electronic Design,* 10/3/94, p. 38, 3 pp.

Cache profiling and the SPEC benchmarks: a case study. Cache performance can be tuned using cache-profiling techniques with the SPEC92 benchmarks. Alvin R. Lebeck, David A. Wood, University of Wisconsin; *IEEE Computer,* 10/94, p. 15, 12 pp.

Base cell design spawns advanced arrays. A new 20-transistor core cell developed by Motorola in 0.5-µm CMOS provides an estimated 70% gate utilization, compared with 55% in existing gate arrays. Cheryl Ajluni, *Electronic Design,* 9/19/94, p. 178, 2 pp.

Long road to overnight success. Successes and failures of optical storage are reviewed as a lesson for new product ventures. Praveen Asthana, IBM; *IEEE Spectrum,* 10/94, p. 60, 7 pp.

Wireless computing. Several applications—including wireless LAN, WAN, paging, and voice/data cellular—indicate that wireless mobile computing is well on the way. Tomasz Imielinski, B.R. Badrinath, Rutgers University; *Embedded Systems Programming,* 10/94, p. 18, 10 pp.

Quality improvements come slower after ISO. In spite of U.S. advances in quality, including ISO9000, concerns are still being raised. Vanessa Craft, *Electronic Business Buyer,* 10/94, p. 53, 3 pp.

Peripherals

Fast Fibre Channel could redefine local area network, I/O worlds. Fibre Channel, expected to be approved by ANSI, offers the flexibility of networks and the speed of I/O channels at 1 gigabit per second. J. Robert Lineback, *Electronic Business Buyer,* 10/94, p. 41, 3 pp.

Smart controllers speed data moves, trim overheads. Responding to faster processors with wider buses, disk-controller ICs are offering more features and higher data rates. Dave Bursky, *Electronic Design,* 9/19/94, p. 85, 11 pp.

Processors

Resolution of data and control-flow dependencies in the PowerPC 601. To utilize the superscalar capabilities of the PowerPC 601, data and control-flow dependencies must be managed. Terence Potter, Mike Vaden, IBM et al; *IEEE Micro,* 10/94, p. 18, 12 pp.

System Design

Hardware approaches to cache coherence in shared-memory multiprocessors, part 1. Solutions to the cache-coherence problem in shared-memory multiprocessor systems are examined in terms of hardware. Milo Tomasevic, Pupin Institute, Veljko Milutinovic, University of Belgrade; *IEEE Micro,* 10/94, p. 52, 8 pp.

3D optical interconnects for high-speed interchip and interboard communications. Potential for increasing speed and lowering power in high-speed computing is offered by 3D optical interconnects between ICs and boards. Ahmed Louri and Hongki Sung, University of Arizona; *IEEE Computer,* 10/94, p. 27, 11 pp.

Battery considerations for portable systems. Designers are required to understand battery parameters and system parameters, including charging circuits and power supplies, to design current portable systems. Harold Myers, Elpac Power Systems; *Electronic Products,* 10/94, p. 25, 4 pp.

The softening of hardware in embedded systems design. Hardware designers use HDL compilers to implement designs, focusing more on algorithms and less on specific hardware. Robert L. Hoffman, *Electronic Design,* 10/3/94, p. ES-24, 6 pp.

