THE EDITOR'S VIEW

AMD's Quandary: Lead or Follow?

Going Head-to-Head with Intel Is Difficult and Expensive

With its forthcoming K5 processor, AMD has shown it is ready to use its own processor designs to compete with Intel. The K5 is designed to be fully compatible with existing Pentium chips, giving AMD a fast entry into the PC market. But Intel can and will use its dominance of that market to change the ground rules, making it hard for AMD to maintain compatibility. AMD would like to be able to set its own rules, but that would require a bigger investment than simply designing processors.

For example, consider system interfaces. A quick comparison of AMD's K5 with Intel's P6 processor shows that the core CPUs are quite similar, yet the P6 will deliver significantly higher application performance, based on estimates from the two companies. Much of the difference lies in the system interface: the P6 connects directly to an L2 cache in the same package as the CPU while reserving a separate high-performance bus for memory and I/O. The K5, trapped in a Pentium pin-out, has a single, slower bus overburdened with cache, memory, and I/O traffic.

AMD could have designed its own P6-like system interface for the K5; this alternative might have boosted K5 performance close to that of the P6. This strategy, however, would have left the K5 incompatible with existing system-logic chip sets and motherboards, limiting market acceptance of the device. Indeed, NexGen used exactly this design strategy with its Nx586, and that company has been slow to gain design wins outside of third-tier vendors and its investors *(see **0905MSB.PDF**)*.

The K5's Pentium-like bus makes it easy for system vendors to use the AMD chip, but this design prevents the K5 from achieving P6-class performance. AMD will face the same conundrum with K6 and future processors. The company claims that its K7 chip, for example, will match Intel's P7 in schedule and performance, but how can AMD achieve this claim with a previous-generation system interface?

AMD could match Intel's performance if it were to forge ahead with a unique system interface, but then its chips would not fit into the PC infrastructure. One way to solve this dilemma would be to adopt Intel's business model: design and market system logic and motherboards to support a new system interface. This effort would be expensive, particularly if AMD wanted to offer a range of chip sets comparable to those offered by Intel and other chip-set vendors. Also, AMD would then be subject to the same criticisms as Intel, which is often accused of competing with its own customers.

Another opportunity for Intel to set standards is in instruction-set extensions. Intel's most recent attempt in this regard was the infamous Pentium Appendix H, which contains "secret" instructions released only under nondisclosure agreements. These instructions are applicable only to operating systems and offer little or no performance benefit in most situations. So far, no significant PC operating systems are using them.

A bigger opportunity will occur if and when Intel adds extensions to improve native signal-processing (NSP). Such extensions, similar to those in HP's processors *(see **080103.PDF**)*, could appear in versions of Pentium and the P6 next year. These new instructions would deliver a major performance boost for many NSP applications and thus are likely to be used widely.

These instructions cannot be present in the K5, since AMD doesn't yet know what they are. In fact, the company cannot add these instructions to its processors until Intel publishes them, which Intel will delay as long as possible. Assuming that AMD starts to modify its chips as quickly as possible, it still could take a year to design, test, and put the changes into production. During that period, Intel should have a significant marketing advantage.

The biggest battle will come around 1998, when Intel releases the first fruits of its partnership with HP. In addition to x86 compatibility, these chips will contain a whole new instruction set that will take AMD years, at best, to duplicate. AMD instead plans to continue with x86-only chips, hoping the new instruction set flops. It's too early to call this race, but we expect that Intel, as is its wont, will spend megabucks to convince customers that its way is the Right Way.

Other x86 processor vendors—Cyrix, NexGen, and the lot—face these same issues, but AMD's sizable market share is crucial for any attempt to combat an Intel standard. The partnership of AMD and Cyrix on OpenPIC *(see **0905MSB.PDF**)* exemplifies the best strategy: teamwork among Intel's competitors against the common enemy. This strategy could be applied to new system buses, instruction-set extensions, and the like. But this disparate band of competitors is likely to have trouble working together on such critical technologies. If teamwork fails, AMD and the rest may revert to playing follow the leader, leaving them perpetually a year or two