# Most Significant Bits

**Compaq to Buy NexGen Parts**

Catapulting NexGen into the top tier of PC makers, Compaq announced that it will incorporate the Nx586 chip in future system designs. The company stopped short of announcing specific systems using the chip; these will probably debut later this year. Compaq will probably use the 586 to supplement its product line, continuing to purchase the bulk of its processors from Intel and AMD.

Not coincidentally, the deal was announced just days before NexGen filed for a public stock offering. The deal gives the fledgling processor vendor a major boost in credibility; current 586 customers are all small, third-tier players. Compaq owns 11% of NexGen and stands to profit from a public offering. The announcement also emphasizes Compaq's willingness (or perhaps desire) to work with Intel's competitors.

It isn't clear how much this announcement will impact NexGen's immediate prospects. Neither company would discuss the potential volume of processor purchases; previously, NexGen had projected shipments of several hundred thousand parts for 1995. With faster Pentiums, the Nx586, and potentially AMD's K5 and Cyrix's M1 to choose from, Compaq may not put the 586 in its highest-volume products. We expect that all these processors (or, in Cyrix's case, the reduced-cost M1 SC) ultimately will appear in Compaq systems.

In any case, NexGen has gained a major customer. Compaq's endorsement should help the startup make sales to other first- and second-tier players, putting NexGen well on the way to being a top player in the x86 processor market.

**Digital Deploys First 21164 Systems**

Extending its lead with the world's fastest microprocessor-based systems, Digital has announced its first products using the 21164 Alpha processor *(see **081201.PDF**)*. The chip will appear in a variety of servers; workstations will follow later. Volume system shipments are not expected until June; Digital had claimed that the 21164 was in production as of March.

The announcement includes a 250-MHz server with an entry price of $60,000. Larger systems supporting 6 or 12 processors at 300 MHz will vie for mainframe downsizing sales. In this maxed-out configuration, the 21164 delivers 341 SPECint92 (peak) and 513 SPECfp92, far surpassing the performance of the fastest systems from competitors by 2.3× on integer and 1.6× on floating-point.

These systems take advantage of Alpha's 64-bit architecture to support up to 14G of main memory, whereas most other microprocessor-based systems are limited to 4G or less. The increased memory space improves performance on large databases and other enormous applications. These multiprocessor systems start at $100,000.

Digital is certainly justified in charging a high price for such high performance, but the lack of a reasonably priced server or a workstation will keep 21164 volumes low. The new processor opens an unprecedented performance gap against the competition, but few users can afford the new systems. By the time Digital offers lower-priced systems, other vendors will have processors that reduce this performance gap, preventing Digital from using Alpha's superior speed to gain market share.

The 21164 has gained one convert for Alpha: DeskStation Technology (Lenexa, Kan.) has announced its own 21164-based system to supplement its line of MIPS-based PCs. At $15,000 for a high-end configuration, the new Raptor system is aimed at users who are "impatient with the high prices and arrogance of other workstation vendors." Wonder if they have anybody in mind?

**PA-7200 Appears But Is Slower Than Expected**

Not to be lost in the server wars, Hewlett-Packard has rolled out its first systems based on the long-awaited PA-7200 chip *(see **080302.PDF**)*. Although the company announced a design goal of 140 MHz at last year's ISSCC, the first systems are limited to just 100 MHz. At this speed, the chip is rated at 136 SPECint92 (peak) and 221 SPECfp92. This integer rating is actually lower than that of HP's current high end, the 125-MHz PA-7150, although the SPECfp92 score is a bit better.

These performance ratings underscore the failure of SPECint92 to measure memory performance. Although the 100-MHz 7200 is roughly equivalent in integer throughput to the 125-MHz 7150, the new chip has a vastly improved memory bus that delivers more than three times the bandwidth of its predecessor. On applications that overflow the processor's 1M cache, the 7200 delivers significantly better performance than the 7150. Despite the clock-speed problems, HP is moving forward with the 7200 because of this advantage.

Another advantage of HP's new chip is its multiprocessor-ready bus. The new K-Class ("Kittyhawk") servers support up to four processors using this bus with no expensive interface logic. Entry pricing for a single-processor system is $21,270; additional processor boards, containing little more than a 7200 and cache, sell for an exorbitant $10,000 each. (DeskStation's quote seems to apply to HP as well.)

HP hopes to push the 7200 to 120 MHz by summer. Even at that clock rate, the new chip would be far behind the performance mark set by the 21164. By summer, Sun and IBM are likely to be shipping workstations based on UltraSparc and the PowerPC 620 that also

 

outrun the 7200 by a large margin. HP's hopes for getting back into the performance race lie with the forthcoming PA-8000 *(see **081501.PDF**)*, which is not expected to ship in systems until 1Q96.

**AMD, Cyrix Unite on MP Architecture**

Seeking to provide an alternative to Intel's APIC (advanced priority interrupt controller), Cyrix and AMD have banded together to support a new standard called OpenPIC. The new interrupt controller design is a software-compatible successor to Cyrix's SLIC, which supports dual-processor systems. OpenPIC can also be used for dual-processor systems, but it is more complex than SLIC and can support up to 32 processors.

The OpenPIC standard is endorsed by Compaq, which doesn't want to be locked into Intel's microprocessors for its multiprocessor server designs. Compaq would presumably like to build multiprocessor servers that could use Pentium, K5, M1, or Nx586 processors.

Unlike Intel's APIC, which consists of one module integrated into each microprocessor and another module integrated into the system logic, the OpenPIC interrupt controller is implemented entirely in the system logic. This allows it to be used with any microprocessor—even an Intel processor, in which case the APIC would be ignored. It could also be used with PowerPC processors.

Cyrix and AMD expect several chip-set makers to include OpenPIC support in their future products. So far, Opti and ALI have publicly committed to do so. Phoenix Technologies will provide BIOS support.

The need for the companies to deviate from Intel's APIC scheme is driven by patent concerns. The chip-level patent claims are not an issue, since AMD has an Intel patent license and Cyrix uses licensed foundries. The concern is with system-level patent claims, for which the chip makers generally do not have licenses. Cyrix and AMD believe that Intel has patents that could be used to demand royalties from a system maker using a non-Intel processor with an APIC. For this reason, neither company chose to integrate the APIC in their Pentium-class processor.

Deviating from Intel's standard creates a software support issue, however. For each different multiprocessor system architecture, a different HAL (hardware abstraction layer) is needed for each OS. All the major OS vendors will supply this support for Intel's APIC-based MP specification. AMD and Cyrix are currently working on a prototype OpenPIC HAL for Windows NT. It will take some time for the OpenPIC standard to develop the widespread OS support expected for Intel's APIC, but if companies like Compaq build servers based on this design, the support will come.

Had AMD and Cyrix each gone their separate ways, the fragmentation would have limited the amount of software support. Now, OS vendors can support the Intel standard and the AMD/Cyrix standard and know that they have the world covered. The OpenPIC architecture specification is available now; send e-mail requests to *openpic@amd.com*.

AMD and Cyrix have been meeting for some time to explore areas of common interest, and future joint standards are likely. One possibility is a multiprocessor system bus to provide an alternative to the standard that Intel will be setting with the P6 bus.

**Intel Processors to Move to 2.5 V**

In 1996, high-end versions of Pentium and the P6 will move to a 2.5-V version of Intel's new 0.35-micron process, increasing clock speeds while reducing power consumption. Intel recently described two versions of the new process. The first is the 3.3-V BiCMOS process used for the 120-MHz Pentium *(see **090403.PDF**)* and future chips that may reach 150 MHz. This version retains compatibility with both the 3.3-V supply used in current Pentium systems and the bipolar transistors in the P54C circuit design.

For new designs, Intel has implemented a pure CMOS version of the 0.35-micron process. Eliminating bipolar transistors saves four mask steps out of 20, a significant cost reduction. The company says that, at 0.35 microns, bipolar transistors add little performance. Reducing the power supply to 2.5 V allows Intel to trim the gate-oxide thickness by 15% to just 60 Å, improving transistor switching speed.

The company confirmed that the P6 will migrate from the current 2.9-V 0.6-micron BiCMOS process to the 2.5-V CMOS process in 1996. We estimate that the new process will boost the P6 clock speed to 200 MHz. Sources indicate that the 2.5-V process will also be used on the unannounced P55C processor, a modified Pentium that will probably include 32K of cache and other enhancements and operate at 150 MHz or beyond.

**Intel Finds More Pentium Bugs**

As promised, Intel has released an update to its Pentium errata lists *(see **090303.PDF**)*. It must have been a busy month for Intel, as the company published 10 new bugs plus a specification change. Two of the bugs are apparently not completely new, as they were known to Intel in time to be fixed in the recent C2 stepping of the P54C. At least six of the remaining problems, however, will require changes in a future stepping.

The specification change increases the maximum $V_{CC}$ to 3.6 V for 100-MHz P54C parts. Previously, standard parts operated at 3.135 V to 3.465 V, but Intel is also shipping "VRE" versions that require a higher voltage range (3.3 V to 3.6 V) to achieve 100-MHz operation. The VRE rating allows Intel to ship parts that can't quite reach 100 MHz at the standard voltage. Some users have been concerned that, when swapping processors, they

 

might plug a standard Pentium into a VRE socket and damage the chip by long-term exposure to the higher voltage. The new specification alleviates this concern.

One of the new problems may impact application software. The CMPXCHG8B instruction, new in Pentium processors, can cause an invalid opcode trap when the instruction is spread across a page boundary and there is a page fault on the second page; the correct operation would be a page-fault trap. This bug could crash software that has been optimized for Pentium processors. It will be fixed in a future stepping.

Most of the other problems involve dual-processor configurations or the APIC. These bugs can all be remedied by changes in the system hardware and should not impact end users. At least two of these bugs occur only with certain third-party chip sets.

If Intel's intention in publishing its errata list is to prove that microprocessors aren't perfect, it is doing a fine job. Although the C2 stepping initially appeared clean, it now is clear that the bugs in that design simply hadn't been disclosed yet. The good news is that there is nothing in the new list that approaches the magnitude of the FDIV problem. Until other vendors step forward with their own bug lists, we must assume that Pentium is no worse than other commercial offerings.

**Motorola Extends 68302 Line**

Three new derivatives of the popular 68300 embedded microcontroller are now available from Motorola, each aimed at a different segment of the intelligent communications peripheral market. The three chips add and subtract features from the basic 68302 (see MPR 10/89, p. 1), offering higher and lower price points. All three chips now have a static 68EC000 core and new low-power operating modes.

The 68LC302 is the least expensive member of the family, with only two serial ports (instead of three) and four DMA channels. The part is intended for modem applications that need two serial ports, one for the host and one for the telecom connection. The LC302 is priced at $11.25 in 10,000-unit quantities, about 25% lower than the vanilla 68302.

A PCMCIA slave interface, a 16550-compatible serial port, and a flat package make the 68PM302 attractive for plug-in card designs such as wireless modems and network adapters. The new features add a 25% premium to the PM302's price tag.

The new top of the 68302 line is the 68EN302, which includes all the basic 68302 features plus Ethernet support and a DRAM controller. By adding 10-Mbps support to what was previously the low-end 68302 controller, Motorola fills the gap below its much pricier 68360 QUICC chip. The EN302 is priced at $25, nearly twice as expensive as the 68302. The EN302 won't be available until 3Q95; the other two parts are shipping now.

**AMD Expands 29000 Line with Printer CPU**

Seeking to entrench itself more deeply in the low-end of the laser and ink-jet printer markets, AMD has developed the new 29202 specifically for printers supporting the Windows Printing System (WPS). The new chip bears a strong similarity to the 29200, but those features not required for WPS are stripped off to save cost. At $15 in quantity, the 29202 is positioned between the low-end 29205 and the more powerful 29240 and 29245.

With an on-chip DRAM controller and an IEEE-1284 enhanced parallel port, the chip is able to drive a 600-dpi WPS printer at 4–12 ppm using only 1M of DRAM. Samples of the 12.5-MHz 29202 are available now, with production scheduled for June.

**Hyundai Enters Multimedia Market**

Hyundai Digital Media (HDM), a newly formed division of Korean manufacturing giant Hyundai, has announced its first product since the division formed last July. The new chip is an intelligent MPEG-2 decoder aimed at set-top boxes and video-on-demand applications, offering virtually all the necessary functions in one chip.

The HDM8211M chip is internally powered by a 32-bit MicroSparc controller; Sun licensed to Hyundai the processor's Synopsys database. The CPU oversees all data transfers, moving MPEG-2–formatted data from the chip's input ports to an external DRAM array, and from the DRAM to the audio and video decoders. A typical configuration requires 2M of DRAM for acceptable MPEG-2 performance.

Most audio and video decoding is performed by on-chip function units supplemented with firmware routines. The SPARC core basically acts as a DMA controller and cannot address off-chip resources, making the 8211 a slave device. Hyundai claims enough CPU performance remains for the customer to add special features such as error detection and recovery or custom video overlays.

HDM has plans to use its SPARC license to create more intelligent MPEG-2 chips in the future. The '8211 is sampling; production is scheduled for August. In a 208-pin MQUAD package, the chip will sell for less than $60 in volume. This price compares well with MPEG-2 decoders from AT&T and IBM, neither of which includes a host processor.

**Erratum: NexGen to Sell PCI Chip Set**

In our previous issue *(see **0904MSB.PDF**)*, we erroneously reported that only VLSI Technology will sell the forthcoming PCI chip set for Nx586 processors. NexGen will also sell this chip set. ♦

 