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NEC Unveils New MIPS Chip for Nintendo

R4300 Builds on R4200 Design with Simpler Bus, Higher Performance

by James L. Turley

Fueling a strange inversion in the microprocessor industry—where toys and games can pack more processing power than most computers—NEC has unveiled a new 64-bit MIPS chip for the burgeoning video-game market. Although neither company would confirm it, the new chip, which was developed by MIPS Technologies in cooperation with NEC, is the heart of Nintendo's upcoming Ultra-64 (aka Project Reality) home video game.

The new chip is directly derived from the R4200. It boosts performance to 125 Dhrystone MIPS, primarily through a 100-MHz clock, 25% faster than the original R4200, and an improved integer/FP multiplier. A new bus interface makes the part easier to design into low-cost embedded systems, and a small plastic package helps keep the price below $50 in quantity.

The chip combines NEC's experience with low-power microprocessors and its background in consumer electronics. Perhaps taking a cue from a German auto manufacturer, MIPS Technologies has named the new chip the R4300i, the suffix ostensibly standing for "interactive." Maybe the cabriolet version will be available in time for summer.

Huge Volume Potential Looms

The video-game giants have now chosen sides. Sega uses two Hitachi SH7604 chips in each Genesis 32X game adapter; the Sega Saturn (currently available in Japan) adds an SH-1 chip to that pair of processors. Nintendo's new Ultra-64 game will use one R4300 with custom video-generation logic. Between them, Sega and Nintendo have divided the $5 billion U.S. video-game market nearly 50/50, shipping a total of 40 million units according to published reports. Most of those systems are powered by 8- and 16-bit CPUs, contributing greatly to 68000 and 65816 volume. Soon both companies will try to repeat their success by moving customers to a newer platform. Even though the market is no longer wide open, the upgrade path could still be very lucrative.

The coming year should be a good one for MIPS boosters. Last year, approximately 1.5 million MIPS-compatible microprocessors found their way into embedded and consumer-electronics items like network hubs, printers, and television set-top boxes. With Nintendo adopting the R4300, that volume could double or triple, due primarily to one application. Like Hitachi's serendipitous design win at Sega, this one system might catapult the R4300 into one of the top volume spots for 1995, far outselling all other MIPS chips combined.

New Chip Looks Like the Old Chip

The R4300 shares much with the R4200 *(see **070701.PDF**)*, its direct predecessor. The R4200 was developed by MIPS Technologies (MTI) but, unlike most other MIPS designs, was funded entirely by NEC in return for a one-year exclusivity contract (which has since expired). The R4300 was also developed by MTI, with help from NEC, but theoretically is available to other MIPS licensees.

Many space- and power-saving measures first seen on the R4200 also appear on the new chip, including the design of the caches, the 32-entry TLB, and the unified FPU. In fact, the two chips are nearly identical apart from their external bus interface, multiply unit, and manufacturing process. Whereas the R4200 was designed for low-cost PCs running Windows NT (ultimately, a null set), the R4300 was tweaked for graphics performance in embedded applications, which the company hopes will be a more profitable venture.

The initial version of the R4300, which is sampling now, runs at 100 MHz, compared with the R4200's 80-MHz top speed. Because the two chips are so similar, they deliver equivalent Dhrystone performance as a function of clock speed. The R4300's faster top speed allows it to achieve roughly 20% better performance than the R4200, with a similar increase in power consumption. The R4300's improved multiplier will assist some applications, while its narrower, 32-bit bus will slow oth-

ers. In Dhrystone testing, neither of these factors has much of an effect.

New Multiplier Shares Space with FPU

As the block diagram in Figure 1 shows, the R4300 folds the FPU logic and register file into an R4000-style integer unit. The R4200 was the first MIPS chip to use this technique. It saves a considerable amount of datapath logic and shrinks die area, but it sacrifices both integer and floating-point performance. For instance, the entire CPU is tied up during long-latency FP operations, which can take more than 50 cycles to execute.

MTI revamped the combined integer/FP multiplier to ease this problem. The older R4200 design has a Booth multiplier that retires three bits of result per clock cycle, yielding a 13-cycle latency for 32-bit unsigned integer multiply operations. Floating-point multiplies execute slightly faster. The R4300's new multiply unit executes a 32×32 multiply operation in only 5 cycles, whether integer or floating-point. Double precision or 64-bit operations have an 8-cycle latency. With the reduced the latency, the R4300's combined integer/FP core is tied up for shorter periods than that of the R4200.

New Bus Is Easier to Handle

One of the few real changes in the R4300 over its predecessor is a redesigned external system bus. The R4300 cuts the customary MIPS SysAD bus in half, to 32 bits, and simplifies the command bus to just five control signals. Neither the address/data bus nor the control signals have parity bits. A five-wire arbitration mechanism allows the R4300 to coexist with other masters, such as a DMA device. Like its parent, the R4300 has a 16K instruction cache and an 8K write-back data cache that does not snoop. An expanded four-word write buffer reduces the frequency and severity of pipeline stalls.

When the processor initiates a bus cycle, it broadcasts address and control information (read/write, burst/single, and number of words), then samples the bus to make sure the slave device is ready before transferring 1–32 bytes of data. Write transfers proceed at a software-selectable pace; the slave throttles read transfers by asserting and negating an acknowledge signal to indicate that input data is valid.

There are no byte-select outputs; byte and halfword operands are placed on the 32-bit bus according to the low-order address bits. External logic must decode the address and size signals and capture data from the correct byte lanes. Because the R4300 samples the slave status during each phase of the transfer, a slow slave device (or slow decode logic) has plenty of opportunity to extend the cycle to meet its needs—an important feature in cost-sensitive consumer devices.

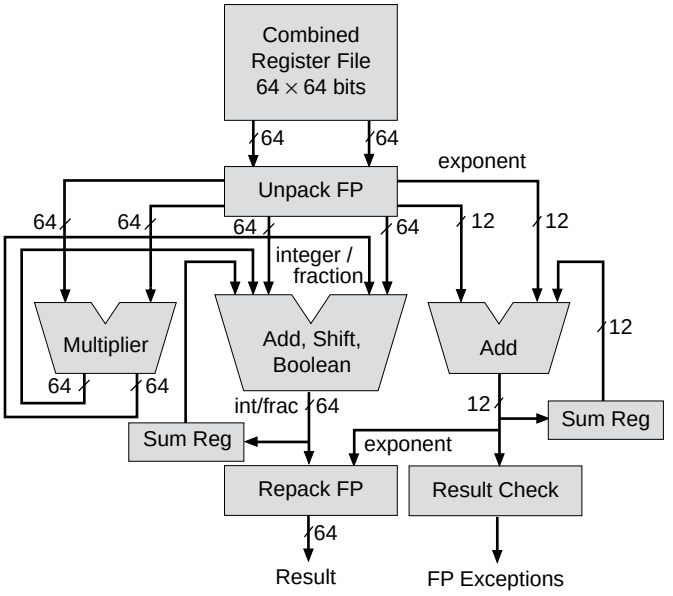

Figure 1. Block diagram of the R4300's mixed integer/FP ALU shows the shared 64-bit data paths between execution units and the combined register file.

Manufacturing Process Saves Space, Cost

The die photo in Figure 2 shows that the R4300 core logic consumes a relatively small part of the die compared with the caches and the TLB. This is an increasingly common situation as processor cores get smaller and instruction bandwidth becomes critical to achieving competitive performance. The R4300 is fabricated on the same line as the R4100 and the 200-MHz version of the R4400, using a state-of-the-art 0.35-micron process with three metal and two poly layers. With the volume represented by the Nintendo design win, NEC was prudent in deciding to manufacture the R4300 in the smallest possible process to get the lowest per-piece price, and to amortize the high initial cost of the process over the life of the part.

The MDR Cost Model predicts a manufacturing cost of $15 for the R4300, about halfway between the costs of the R4100 and the R4200. This cost is equivalent to that of the Hitachi SH7708.

NEC is now sampling R4300 chips at 100 MHz, with production in September. A faster version is likely to follow by a few months, based on NEC's success in building the 200-MHz R4400.

Clock Manipulation Now Commonplace

The R4300 uses clock multiplication to achieve its fast pipeline rate while maintaining a reasonable bus frequency. The external bus runs at the frequency of the input clock, which must be in the range of 10–67 MHz. The pipeline clock may be multiplied by 1×, 1.5×, 2×, or 3×, relative to the input/bus clock, up to a maximum of 100 MHz. The multiplier is selected during power-up initialization via two external pins.

The best performance is obtained with a 67-MHz bus clock with the core running at 1.5×. Typical power dissipation in this mode is 1.8 watts. The bus can run as slowly as 33 MHz using the 3× multiplier before it impacts the internal pipeline frequency.

As in the R4200, a standby mode is enabled by a control bit in the processor. Standby mode divides all clocks by four, so an R4300 at top speed drops to 25-MHz internal/16-MHz external. Power falls to about 450 mW.

The minimum speed of the pipeline is limited to 20 MHz; the R4300 is not static. To stop the processor clock entirely, all the registers must be saved to nonvolatile storage and restored when the processor starts again. All cache contents are lost. Although NEC has taken measures to keep power consumption reasonable, the company does not think that completely powering down the processor is crucial for the target applications, which will be line-powered.

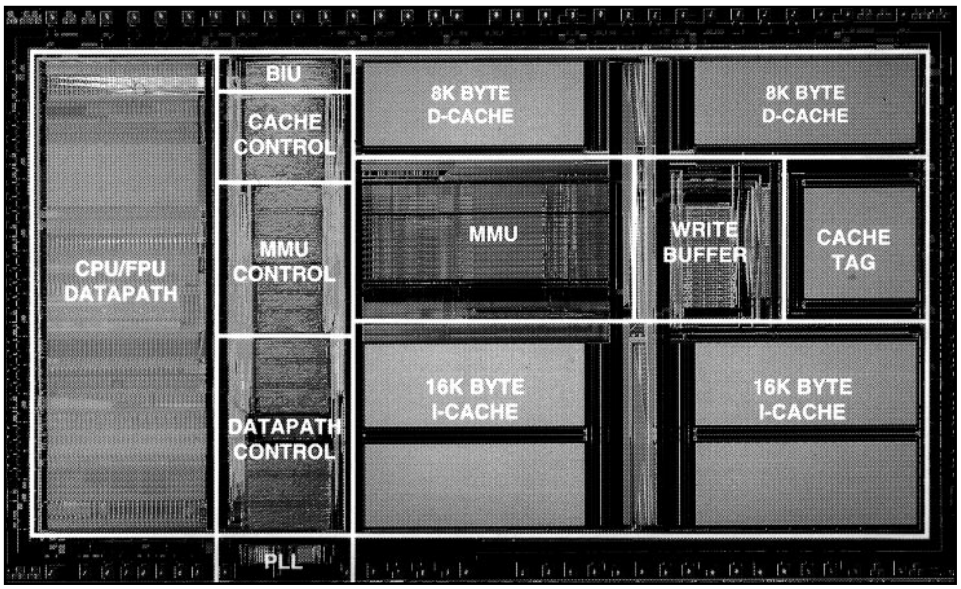

Figure 2. A die photo of NEC's R4300 shows that the dual cache arrays and MMU overwhelm the small MIPS-III core. The die measures approximately 8.6 mm by 5 mm in NEC's 0.35-micron process. Using a 4T SRAM cell, the chip includes nearly 1.7 million transistors.

Performance Tops Embedded Charts

The chip's simulated performance of 125 Dhrystone 2.1 MIPS at 100 MHz puts it near the top of the crop of embedded microprocessors, as Table 1 shows, and rivals all but the fastest Pentium chips.

In integer performance, the R4300 stands astride Intel's top 960-family parts, the 50-MHz 960HD and the 75-MHz 960HT. Like the R4300, the 960 chips have a 16K I-cache and an 8K D-cache, clock multiplication, and a 32-bit external bus. Given the chips' identical cache structures and similar bus bandwidth, Dhrystone results should be somewhat more accurate than usual when comparing the MIPS and 960 families. Because the 960HT is superscalar and uses a more powerful instruction set, it has an advantage over the scalar MIPS design, delivering the same performance at 75 MHz that the R4300 delivers at 100 MHz.

Figure 3 shows how the R4300 stacks up on both integer and floating-point performance against other RISC chips on the larger SPEC92 suite. The new design's gain over the R4200 is a combination of its faster clock rate and its new multiplier, offset significantly by its narrower 32-bit bus.

Although the clock rate increases by 20% from the R4200 to the R4300, integer performance grows by less than 10%, according to the company's estimates. These results underscore how the SPEC benchmarks are much more sensitive to memory bandwidth than are simpler, cachable benchmarks like Dhrystone. Floating-point performance, in contrast, jumps by 50% due to the R4300's much-improved multiplier, which is used more heavily in FP tasks.

For some applications, the R4300's big advantage over its competitors will be its internal floating-point support. Even with it, the chip dissipates far less power than either of the two Intel chips, which are fabricated with a 0.5-micron (drawn) gate length in Intel's more power-hungry BiCMOS process.

The R4300 is also much less expensive, with a 10,000-piece price of $45 compared with Intel's $125 price for the 960HD, or more than $155 for the faster 960HT. The price is in line, however, with Hitachi's goal of about $50 for the 100-MHz SH7708.

	R4300	SH7708	960HD	960HT	602
Frequency	100 MHz	100 MHz	50 MHz	75 MHz	66 MHz
I-Cache	16K	8K	16K	16K	4K
D-Cache	8K	Unified	8K	8K	4K
FP Support?	Yes	No	No	No	Yes
Bus Width	32 bits	32 bits	32 bits	32 bits	64 bits
Transistors	1,700,000	800,000	2,300,000	2,300,000	1,000,000
Die Size	45 mm^2	44 mm^2	100 mm^2	100 mm^2	50 mm^2
Voltage	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
Power (typ.)	1.8 W	0.7 W	3.0 W	3.0 W	1.2 W
Dhry. MIPS	125	100	83	125	65*
Est. Mfg. Cost*	$15	$12	$50	$50	$14
List Price (10K)	$45	$50	$125	$158	$45*

Table 1. A comparison of the R4300 with Intel's 960, the PowerPC 602, and Hitachi's SH-3 processor shows that NEC's chip delivers competitive performance and power consumption and adds FP support that the expensive chip lacks. (Source: vendor data except *MDR estimates)

Similar price and similar performance will make the SH7708 and R4300 fierce competitors (outside of the video-game arena, of course, where the victors are already known). Hitachi opted for a much smaller, unified cache in the 7708 and an even smaller one in its SH7702 sibling, while NEC splurged. The two parts' die sizes are nearly identical, however, due to NEC's smaller process and careful packing of the design. NEC's 3Q95 production schedule for the R4300 is 3–9 months ahead of expected availability of 100-MHz SH7708 chips.

The R4300's floating-point functions and larger caches are significant free bonuses over the 7708. The cachet of MIPS software compatibility and established tools may also attract designers with an eye toward upgrading in the future. On the other hand, the Hitachi instruction set produces smaller object code than MIPS, saving on ROM and RAM and alleviating some of the effect of the 7708's smaller cache. In test situations, the space savings can be as much as 30%, according to Hitachi.

While the R4300 is no wastrel with electricity, it is not suitable for handheld applications that rely on battery power for long periods of time. The SH7708 consumes less than half the power of the R4300 and delivers up to 80% as much integer performance. The Hitachi part can also operate with a 2.5-V supply, pushing current consumption down further. Limiting power consumption was not NEC's intention; for line-powered consumer products, total power dissipation must only remain below a certain threshold to avoid adding a fan. Dropping power any further (as with clock-stopped operation) buys nothing.

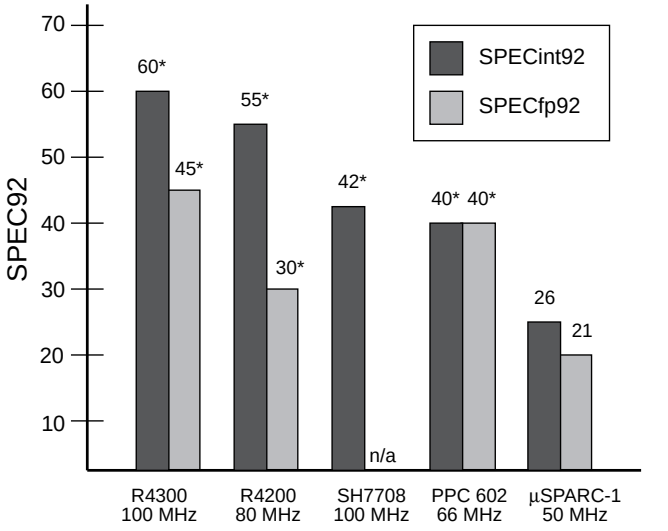

Figure 3. Estimated and actual SPEC numbers reveal the R4300's basis in the R4200 design. The slightly lower SPECint92/MHz ratio for the R4300 is due to its narrower system bus. (Source: SPEC except *vendor estimates)

Price & Availability

Samples of the 100-MHz R4300 are available now from NEC in a 120-lead PQFP for $50. Production is scheduled to begin in September. The 10,000-piece price for the part is $45. For more information, contact NEC Electronics (Mt. View, Calif.) at 800.366.9782; fax 800.729.9288.

Consumer Electronics Booming

NEC is only one example of a number of microprocessor vendors chasing the elusive goal of a truly high-volume design win in consumer electronics. More and more, the term "embedded processing" doesn't stand for industrial control, office automation, or telecommunications infrastructure. These are all technical applications for technical or professional users. The real volume is now in applications for the average person. The performance of new 32-bit and 64-bit microprocessors enables entirely new products that are becoming "must-haves" for the masses.

The growth of video games, satellite receivers, cable-programming decoders, and other electronic entertainment items is changing the focus of many microprocessor vendors. These applications all deal in graphics, video, and large data sets, requirements that demand a high-bandwidth bus and top-notch integer and/or floating-point multiply performance. Yet the price must be minimal, the production stable, and the power dissipation low enough to minimize heat. For those companies that can meet these considerable challenges, the rewards can be great, indeed. ♦

