Patent Watch

by Rich Belgard, Consultant

The following U.S. Patents related to microprocessors issued recently:

5,398,328
System for obtaining correct byte addresses by XOR-ing two LSB bits of byte address with binary 3 to facilitate compatibility between computer architectures having different memory orders
Issued: March 14, 1995
Inventors: Weber, Larry B., et al
Assignee: Silicon Graphics
Filed: September 27, 1983
A method and apparatus for enabling a computer to run using either a big-endian or little-endian architecture is provided. The method and apparatus use the fact that XOR-ing the lower two bits of a byte address in one architecture with a binary 3 converts that byte address to the equivalent byte address in the other architecture. The conversion method and apparatus is implemented in hardware by setting a bit in a status register indicating a big-endian or little-endian architecture in conjunction with an XOR gate which couples the byte address to binary 3.

The conversion method and apparatus is implemented in software by scanning the instructions of the input for load and store instructions. The software modifies the instructions by taking the contents of the register and XOR-ing the two least significant bits of the byte address with a binary 3.
Claims: 9

5,398,321
Microcode generation for a scalable compound instruction set machine
Issued: March 14, 1995
Inventor: Jeremiah, Thomas L.
Assignee: IBM
Filed: January 21, 1994
An apparatus for generating microcode operates in response to compounding information indicating that two or more adjacent instructions are to be executed in parallel. Separate and independent microcode is held in control store for each possible instruction in a group. Microcode sequences for each instruction of a group of instructions to be executed in parallel are merged in response to the compounding information into a single microinstruction sequence.
Claims: 9

5,398,319
Microprocessor having apparatus for dynamically controlling a kind of operation to be performed by instructions to be executed
Issued: March 14, 1995
Inventors: Sakamura, Ken, et al
Assignee: Sakamura, Ken; Hitachi
Filed: September 11, 1992
A microprocessor including instruction-decoding apparatus, instruction-execution apparatus and information-holding apparatus. The microprocessor performs a first step of storing information specifying the kind of operation to be performed by the instruction-execution apparatus, upon execution of a first instruction, in the information-holding apparatus and a second step of causing the instruction-execution apparatus to perform the kind of operation specified by information stored in the information-holding apparatus when a second instruction is decoded and includes information specifying that the operation to be performed by the instruction-execution apparatus is the kind of operation specified by the information stored in the information-holding apparatus.
Claims: 22

5,396,634
Method and apparatus for increasing the decoding speed of a microprocessor
Issued: March 7, 1995
Inventors: Zaidi, Syed A. A., et al
Assignee: Intel
Filed: September 30, 1992
Apparatus for increasing the decoding speed of a microprocessor. A first decoder generates a single initial microinstruction vector from simple macroinstructions and from complex macroinstructions having a beginning microinstruction equivalent to a microinstruction for a simple macroinstruction. The first decoder also includes apparatus for indicating a beginning address for generating any remaining microinstruction vectors for a complex macroinstruction decoded by the first decoder. The apparatus also includes apparatus, coupled to the first decoder, for generating any remaining microinstruction vectors for complex macroinstructions decoded by the first decoder. The apparatus for generating any remaining microinstruction vectors includes apparatus for responding to the apparatus for indicating a beginning address.
Claims: 3

Other Issued Patents
5,396,611 *Microprocessor use in in-circuit emulator having function of discriminating user's space and in-circuit emulator space* ♦

