UltraSparc Rolls Out at Target Clock Speed

Sun Also Announces High-Performance Chip Set

by Linley Gwennap

Hoping to erase SPARC's performance problems, Sun's SPARC Technology Business (STB) has officially announced its UltraSparc processor at a clock speed of 167 MHz. Although the clock speed is on target, the integer performance of the chip, an estimated 240 SPECint92, is 15% below the original 275-SPECint92 goal. The estimated FP rating of 350 SPECfp92, on the other hand, is significantly better than expected.

The new processor is currently sampling, and STB expects to begin volume shipments in 4Q95, a quarter later than in previous plans. Sun has not yet announced any UltraSparc systems. STB has put a premium price on its new device: $1,595 in quantities of 1,000 for the 167-MHz version.

The company recently revealed extensive details about UltraSparc's system interface, along with a chip set that will allow other companies to build UltraSparc systems with competitive performance. The processor and chip set support a sustainable memory bandwidth of 1,333 Mbytes/s, more than twice that of the P6 *(see **090701.PDF**)*, using a 128-bit bus running at 83 MHz.

Chip Set Allows Complete Workstation

Sun has traditionally withheld system components from partners to keep them from matching Sun's own systems at first release. STB is changing the rules with UltraSparc, announcing a complete system-logic chip set and reference design six months before Sun itself expects to ship systems. The chip set, as Figure 1 shows, provides a complete uniprocessor workstation system.

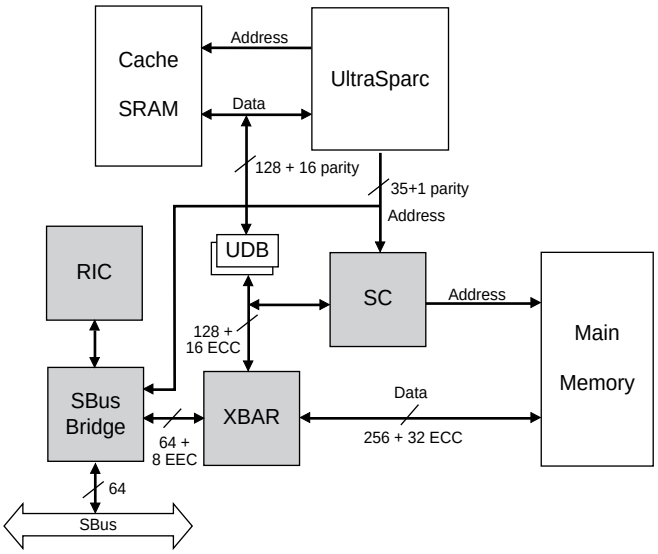

Figure 1. The UltraSparc chip set includes the system controller (SC), SBus bridge, RIC, and crossbar (XBAR) chips.

The key component is the system controller (SC). This device implements a complete memory controller and controls access to the bus. The chip set also includes an SBus bridge chip; STB supplies a variety of products (not included in the UltraSparc chip set) to provide graphics, networking, and other peripheral functions from SBus. The RIC handles interrupts, clock control, and other system functions. Finally, the bit-sliced crossbar (XBAR) chips decouple the very wide memory bus from the I/O bus, allowing transfers to occur in parallel.

The chip set is built by AT&T, except for the XBAR chip, which Texas Instruments fabs. TI also builds the UltraSparc CPU. The chip set, like the CPU, is sold only through STB and is priced at $450. A complete UltraSparc system can be built from less than $2,000 of VLSI chips from Sun, plus memory and other components.

Multiple Buses Deliver High Bandwidth

As the figure shows, even this basic UltraSparc system uses a number of decoupled buses. Secondary cache traffic is handled by a 128-bit data bus that runs at the speed of the CPU *(see **081301.PDF**)*. Two external buffer chips (UDB), which add $170 to the processor cost, connect this bus to a lower-speed system bus that runs at a maximum of 83 MHz (one-half the speed of the 167-MHz processor). The system bus is also 128 bits wide, giving it a peak bandwidth of 1,333 Mbytes/s.

For memory transactions, the CPU sends an address directly to the system controller (SC). The SC, which controls the memory system, fetches the requested data and returns it to the UDB, which passes it to the CPU. With 60-ns DRAMs, it takes 28 processor cycles from the time that the CPU detects an L2 cache miss until the critical word is available to the CPU.

If the transaction is a write, the CPU transfers the data to the UDB (at the CPU clock speed) at the same time that it writes the address to the SC. The SC then reads the data from the UDB before writing it to memory.

The UltraSparc system bus uses a split-transaction protocol. Once the initial request is made to the SC, the bus is free for other transactions. After the SC reads the data from memory, the data must wait for access to the bus before going back to the CPU.

A uniprocessor system can take advantage of the split-transaction bus during heavy graphics work. As the

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figure shows, the crossbar (XBAR) chips isolate the memory bus from the I/O bus. Instead of stalling during the latency of a memory read, the processor can write data to the graphics system or other I/O devices. The UltraSparc processor can have only one pending read transaction on the bus, but it allows several I/O writes as well as a single memory writeback to be in progress at the same time.

The crossbar also simplifies the design of I/O devices. The main I/O bus is 64 bits wide, so high-speed I/O devices don't have to support the 128-bit-wide system bus. A separate chip provides a bridge to a 64-bit SBus, where standard low-cost peripherals can be added. Sun is developing graphics interfaces for the main I/O bus, but these are not yet available from STB.

Finally, the crossbar helps reduce the number of devices on any given bus and hence the bus length. With a relatively short bus, Sun can achieve its 83-MHz bus clock using standard 3.3-V CMOS signals. In contrast, the P6 is specified at only 66 MHz despite using special GTL+ signal levels *(see **090701.PDF**)*. Sun rejected GTL for UltraSparc to avoid the need for special power supplies and termination circuitry, instead relying on mainstream, high-volume components.

Adding Bandwidth for Multiprocessors

The UltraSparc bus design is well suited to multiprocessor systems, although STB has not yet announced an MP chip set. In an MP system, the SC would act as a central arbiter for memory and I/O devices, while the processors arbitrate among themselves to obtain the single address bus. The SC would also decide which devices have access to the data bus on each cycle.

With separate signals for arbitration, address, and data, UltraSparc can fully pipeline transactions. For example, read requests, which don't use the data bus, can overlap read responses, which don't use the address bus. The split-transaction protocol allows transactions to complete out of order, which helps keep the bus at peak efficiency. Each processor, however, always sees its read transactions complete in order, simplifying software.

With multiple processors, it is easier to fill the bus bandwidth. In fact, the UltraSparc bus can sustain its peak bandwidth of 1,333 Mbytes/s for an indefinite sequence of read (or write) transactions. A dead cycle is required between reads and writes to turn the bus around; thus, for realistic sequences of transactions, the maximum bandwidth will be somewhat less than the peak rate. Figure 2 shows a sequence of overlapped transactions that comes close to fully utilizing the data bus.

MicroSparc-2 Hits 110 MHz

STB also announced a new speed grade of its low-end MicroSparc-2 processor. Previously available at 70 and 85 MHz, the chip is now shipping at 110 MHz as well. The new speed grade replaces the old 100-MHz version, which was announced for 3Q94 shipments *(see **0804MSB.PDF**)* but never shipped. The new version uses Fujitsu's 0.4-micron process, also used in Ross's latest HyperSparc chips, to achieve the higher clock rate; the 0.5-micron process used for the slower chips did not produce adequate yield at 100 MHz. The 110-MHz part is otherwise identical to other MicroSparc-2 parts.

In Sun's SparcStation 5 Model 110, the new processor delivers 79 SPECint92 and 65 SPECfp92. With 32M of memory, a 1G hard disk, and a 17" color monitor, the Model 110 sells for $9,595. The chip itself lists for $649 in 1,000-piece quantities from STB. The price of the 85-MHz version has been cut to $415, while the 70-MHz part is only slightly less at $379.

As the figure shows, UltraSparc processors can assert an address immediately after the arbitration cycle; the P6, for example, requires an extra cycle for arbitration. To speed uniprocessor systems, UltraSparc supports bus parking, eliminating the arbitration delay entirely.

Addresses are placed on the bus in two cycles, with the most-significant 36 bits in the first cycle and the remaining 5 bits in the next cycle. The total physical address space is an enormous 512G, divided equally between memory and I/O. With split transactions, the time between the address being sent and the data response is arbitrary and entirely a function of system design.

UltraSparc processors maintain full cache consistency by snooping the bus. The protocol supports cache-to-cache transfers if a snoop hit occurs, but the memory does not "snarf" the data as it is transferred. The timing for cache-to-cache transfers is roughly the same as for memory-to-cache transfers.

For high-end MP systems, the system bus itself could be split into multiple segments, providing more parallelism. Such a design would require a more complicated system controller and crossbar, but it would deliver

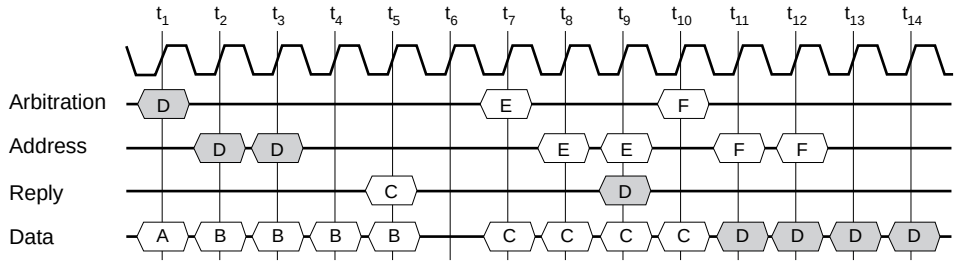

Figure 2. The UltraSparc bus uses a split-transaction protocol with no fixed latency between requests and responses. Transactions A and B are back-to-back read transactions, while C and D are back-to-back write transactions. One dead cycle is required between reads and writes.

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Data General Finds SPARC

As the last major proponent of 88000-based systems, Data General has for years been searching for a processor architecture with a future growth path. The company recently announced that it will port its DG-UX operating system to SPARC, increasing speculation that the company would market SPARC-based systems as soon as 1996. Sources indicate, however, that Data General continues to evaluate other processor architectures, including x86, and has not yet selected SPARC as the successor to the 88000 in its hardware portfolio.

The SPARC version of DG-UX will be offered to both Sun and Data General customers. The port, due in 1H96, will support SPARC V9's 64-bit extensions, and it may be the first 64-bit operating system available for SPARC. The effort to make the port is considered minor, due to portability features already included in DG-UX. Thus, with little effort, the new OS could suit the needs of some high-end customers, but it may not indicate a new strategic direction for Data General.

Price & Availability

The UltraSparc processor and data-buffer (UDB) chips are now sampling; the UltraSparc chip set is expected to sample in June. These products are all scheduled for volume shipment in 4Q95.

The UltraSparc processor sells for $1,595 at 167 MHz or $1,095 at 143 MHz. The UDB lists for $85, while the UltraSparc chip set is priced at $450, all in quantities of 1,000. For more information, contact SPARC Technology Business (STB) at 408.774.8545 or access the World Wide Web at *http://www.sun.com/stb*.

high throughput with four or more processors.

This switched bus design improves system performance by allowing multiple bus transactions to occur in parallel. Each bus can be optimized in width and clock speed to meet the bandwidth and cost demands of individual devices. Performance can be scaled indefinitely by adding more buses. The downside is the complexity of the system-logic chip set, particularly the SC.

UltraSparc Pricing Competitive

While STB charges a premium price for the 167-MHz UltraSparc, the company also offers a 143-MHz version with a more reasonable $1,095 tag. (Note that these clock speeds equate to 6-ns and 7-ns cycle times, respectively.) With the two required UDB chips, however, the total price of the slower part is $1,265. Since this chip should deliver about 205 SPECint92, its price/performance works out to $6.17 per SPECint92.

The 143-MHz chip's price compares favorably with that of Sun's SuperSparc; indeed, the 75-MHz SuperSparc-2, which delivers only 120 SPECint92, is priced at $1,080. Including a $399 cache controller, SuperSparc-2 carries a higher price than UltraSparc but delivers much less performance at a cost of $12.35 per SPECint92. Given this pricing structure, STB expects all new system designs to use UltraSparc instead of SuperSparc-2, leaving the latter chip for legacy designs and MBus upgrade modules only.

STB likes to compare UltraSparc's price with the whopping $2,936 tag hung on Digital's 300-MHz 21164, but that processor delivers 40% more performance than the Sun design. Digital's 275-MHz 21064A produces nearly the same SPECint92 as the 143-MHz UltraSparc, costs $1,188 in similar quantities, and is shipping today. RISC chips such as the R4700 and PowerPC 604, while not in the same performance class as UltraSparc, are rated at less than $4 per SPECint92.

UltraSparc will also have to contend with Intel's P6, as both are due in systems at about the same time. We project that UltraSparc will deliver about 20% more integer performance than the P6 at about the same price. The P6 price, however, includes 256K of fast secondary cache, which roughly levels the price/performance field. UltraSparc should deliver much better floating-point and multimedia performance than the P6, and its faster bus should give it an edge for servers.

In summary, UltraSparc's price/performance is a big step forward from the uncompetitive SuperSparc family. The 143-MHz part is priced competitively with other high-end processors but does not significantly improve on their price/performance. STB is charging a stiff premium to upgrade to 167 MHz, a price that is not justified unless customers are locked into the SPARC architecture. The company hopes that existing customers will be willing to pay big bucks for a chip that doubles the performance of the existing top of the line.

Even if UltraSparc is worth its premium price, it still does little to alleviate SPARC's performance problems in the critical $500–$900 space, where STB continues to rely on its weak SuperSparc line. The most important measure of cost is how SMCC will price UltraSparc workstations, a value that remains to be seen.

The good news is that the fast processor puts SPARC back in the performance race; we expect UltraSparc systems, assuming they ship in 4Q95 at 167 MHz, to exceed all processors except the 21164 in integer performance. But the R10000 and PA-8000 are both due in 1Q96 with 30–50% better projected performance than UltraSparc. Sun is already working on a faster processor of its own and hopes to at least trade performance leads with its rivals rather than being mired in the back of the pack. By combining the new CPU with a high-bandwidth system design, UltraSparc boosts Sun's prospects for both workstations and servers. ♦

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