Most Significant Bits

K5 Hits Speed Bump, May Ship at 75 MHz

Just weeks after announcing that K5 shipments had slipped into the fourth quarter *(see **090602.PDF**)*, AMD chief Jerry Sanders stated that these Q4 parts would run at just 75 MHz, significantly below their frequency target of 100 MHz, although he stopped short of an official product announcement. Sanders also demonstrated working K5 systems running popular Windows programs; these systems ran at 50 MHz.

Granting AMD's yet-unproven assertion that the K5 will deliver 30% better performance than a Pentium at the same clock speed, these parts would be in the performance range of a Pentium at 90 to 100 MHz. MDR projects that in 4Q95, a 90-MHz Pentium will have a list price of about $300. As a second-tier supplier, AMD will need to price a 75-MHz K5 at perhaps $250 to be competitive. Yet the MDR Cost Model calculates that the initial K5 chips will cost roughly $175 to produce, making the 75-MHz device a poor profit maker.

AMD notes that it has done little speed tuning on the initial parts, instead focusing on verifying functionality. Indeed, the company has little motivation to tune the 0.5-micron die, which will be used for Q4 shipments, since it will be superseded by a 0.35-micron version in early 1996. With higher performance and an estimated manufacturing cost of $125, the smaller part will deliver much better profitability than the initial version.

AMD hints that the 0.5-micron design may run faster than 75 MHz, and the company stands by its goal of 133 MHz "and beyond" for the 0.35-micron design. We believe these goals are aggressive. As we pointed out when the K5 was first revealed *(see **081401.PDF**)*, AMD's processor is the only pipelined x86 design to squeeze the memory-address generation and data-cache access into a single clock cycle. The company combined these functions in one cycle to keep the K5 pipeline short despite extra decoding overhead, but this decision may drag down the clock speed.

It could take a lot of circuit work to get clock speeds from the demonstrated 50 MHz to even 75 MHz, and more than a process shrink will be required to get to 133 MHz. The K5 needs to meet its clock-speed goals to match up with Intel's fastest Pentium processors. Otherwise, the K5 will end up being priced against Intel's midrange Pentium chips, delivering modest but not exceptional profit margins.

AMD Inks Two Deals with HP

HP has broadened its relationship with AMD in two areas. First, AMD will develop new processors, similar to its 386SC chip, for HP's handheld computers. The 386SC, also known as Elan *(see **071404.PDF**)*, combines a 386 CPU core with all the logic needed for a PC/AT-compatible system and can run off two AA batteries. AMD claims several design wins for the 386SC, but no such products have been announced.

The companies are mum about the new processor, but it will likely use AMD's 486 CPU core, improving performance over the current Elan, while enhancing the peripheral set. To reduce cost, AMD will probably build the chip in its 0.35-micron process. AMD will also sell the new device as a standard product, with availability slated for late 1996. HP will use the new devices in palmtop PCs akin to its popular 200LX product. The company is also planning a PDA using the Geos operating system instead of DOS.

Separately, HP's personal computer group has announced that it will begin purchasing some 486 processors from AMD. While vendors such as Gateway and Dell expect to completely phase out their 486 product lines this summer, HP sees strong continuing demand for 486 systems among its customer base, which consists primarily of business users. Intel is aggressively cutting back on 486 shipments *(see **0906MSB.PDF**)*, forcing HP to seek an additional supplier to meet its 486 needs. HP joins Compaq and Digital as leading PC vendors buying AMD processors.

Ironically, both HP and Compaq are using AMD's processors in products aimed at home users while relying on Intel 486 chips for their business customers, who are more picky about processor brand names. In the short term, the AMD shipments will help HP steer its Intel processors to its business products. But with consumer interest in the 486 flagging rapidly, it isn't clear how long HP will be interested in AMD's 486 chips.

NexGen Cuts Prices, Signs New COO

As Intel continues its blistering pace of Pentium price cuts *(see **0906MSB.PDF**)*, NexGen has responded with cuts of its own. The latest price adjustments leave the price of a 93-MHz Nx586-P100 at $399, while the low-end 70-MHz version reaches $220. The 75-MHz product is also priced at $220, essentially obsoleting the 70-MHz part; NexGen reports that yield improvements have put nearly all the good chips at 75 MHz or above.

The new prices maintain NexGen's advantage over Intel, based on the company's performance testing. NexGen rates its P100, for example, at the same performance level as a 100-MHz Pentium but sells it for 17% less. Recently, PCs using Intel's Triton chip set have opened a performance gap against NexGen-based systems, which cannot take advantage of standard PC chip sets. NexGen hopes to reduce that gap when it ships its own PCI chip set this summer.

NexGen also lacks a chip that can keep up with Intel's new 120-MHz Pentium, much less the 133-MHz part that we expect to arrive next month. NexGen promises that it too will have faster parts this summer.

The startup company has taken its competition with Pentium to a personal level by signing Vinod Dham as its new chief operating officer, reporting to CEO Atiq Raza. Dham was previously the general manager of Intel's Pentium processor group and supervised the development and launch of that chip. Given his knowledge of the Pentium market, Dham's willingness to move to NexGen speaks well of the tiny company's prospects in the x86 market.

Intel's Enhanced Pentium Slips to 1996

Intel has acknowledged that its much-rumored P55C, an enhanced version of the current P54C Pentium, will not be in production until sometime in 1996 instead of the 4Q95 date we had expected. Intel still plans to ship 150-MHz Pentiums before the end of this year using the 0.35-micron P54CS design *(see **090402.PDF**)*.

The company has not disclosed what enhancements will appear in the P55C, but we expect that it will double the cache sizes of current Pentiums and include some instruction-set extensions for multimedia (although possibly only the conditional-move instruction found in the P6). The new chip will use a 2.5-V version of Intel's 0.35-micron process to exceed 150 MHz in speed, perhaps as fast as 180 MHz.

Siemens to Market MoSys DRAMs

MoSys added a second source for its multibank DRAM (MDRAM) chips by signing Siemens to produce and market the part. Currently, the MDRAM is sold only by MoSys itself, which contracts the actual manufacturing to three unnamed foundries. Siemens will become the fourth manufacturer of the chips and will also market the parts. Neither MoSys nor Siemens has formally announced the price or availability of MDRAM chips. Siemens expects to introduce its parts in early 1996.

MoSys has not released technical specifications for its revolutionary DRAM, which delivers 660 Mbytes/s using multiple banks of memory on a single chip *(see **081002.PDF**)*. MoSys claims that its parts will carry only a 10% price premium over standard DRAMs. The company has not yet announced any design wins, although several graphics vendors are evaluating sample devices. Siemens' endorsement indicates that at least one major memory vendor believes that the MoSys design has the potential to be a high-volume product.

IIT Makes MPEG Authoring Affordable

Bringing MPEG technology to a new price point, IIT has announced a two-chip set that supports MPEG-1 video encoding in real time and connects directly to PCI. While other real-time MPEG encoders cost hundreds of dollars, IIT is pricing its MEP (multimedia encode processor) at $45 in 10,000-unit quantities, plus $18 more for the VPIC (video PCI interface chip). Both chips are currently in production.

The MEP is derived from the company's VCP *(see **0715MSB.PDF**)* by removing H.320-specific logic, the error-correction block, the dedicated Huffman encoder, and a few other features. The new chip is capable of only I-frame encoding, which allows easy editing but creates files 2–3× larger than those using the complete MPEG standard with I/B/P-frame encoding. IIT plans a future software release that will allow the MEP to perform I/B/P encoding, but not in real time.

With its low price and glueless PCI interface, the new chip set is ideal for PC add-in cards, although a separate chip is needed for MPEG audio encoding. At least one vendor, Number Nine, is preparing such an add-in card. Because the MEP also performs MPEG decoding, it can be used for either creating or viewing MPEG video material. IIT is also developing software that will allow the programmable device to perform H.324 encoding and decoding, allowing an MEP-equipped PC to perform video conferencing over standard phone lines. ♦

From the Mailbox

I would like to comment on Brian Case's article about the new "decoupled execution architecture" that makes CISC microprocessors more competitive *(see **0902VP.PDF**)*. I would say that the performance of a microprocessor depends on implementation (or microarchitecture), design optimization, resources, and commitment. The instruction set of a microprocessor, whether RISC or CISC, only plays part of the role.

Design optimization plays a key role in the performance of a microprocessor. The performance and cost of MicroSparc are not as good as those of the 486DX2. Why? Because MicroSparc relies heavily on automatic CAD tools, while the 486 is designed mainly by hand. This full-custom design can achieve a much higher clock rate and smaller die size than a microprocessor designed using semicustom methodology, even though x86 is harder to design than the SPARC architecture.

I don't know whether the inspiration-to-perspiration ratio of a successful microprocessor is 1% to 99% or not. But I do know the architecture doesn't account for 99% of the ingredient. The more I gain complete hands-on experience in the different aspects of microprocessor design, from circuit design, logic design, and architecture definition, the more I feel this way.

—Shine Chung, Principal Engineer
Hitachi Micro Systems

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