## Patent Watch

## by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently:

**5,408,626** One-clock address pipelining in segmentation

unit

Issued: April 18, 1995 Inventor: Dixit, Ashish

Assignee: Intel

Filed: October 26, 1993

Claims: 13

A microprocessor that comprises a three-input adder, a two-input adder, apparatus for providing the components of a virtual address to the first and second adders on a first clock period, apparatus for providing a segment base address to the first adder on the first clock period, apparatus for determining the type of addresses generated by the adders on a second clock period and for generating an output address on the second clock period, and apparatus for determining access violations during a third clock period.

**5,408,625** Microprocessor capable of decoding two in-

structions in parallel Issued: April 18, 1995

Inventors: Narita, Susumu, et al

Assignee: Hitachi

Filed: December 17, 1993

Claims: 3

An instruction fetch unit in a microprocessor, capable of decoding two instructions in parallel, fetches the first and second instructions of the shortest instructions in one cycle. The fetched instructions are decoded by separate instruction decoders. In a case where an instruction longer than the shortest instruction has been fetched by the instruction fetch unit, information to be decoded by the second instruction decoder is the non-head code of the instruction; hence, a pipeline control unit invalidates the decoded result of the second instruction decoder.

**5,404,559** Apparatus for asserting an end-of-cycle signal to a processor bus in a computer system ...

Issued: April 4, 1995

Inventors: Bonella, Randy M., et al

Assignee: Compaq Filed: March 22, 1993

Claims: 7

A modularized computer system based on the 386 or 486 is upgraded to the Pentium processor. The host and I/O buses are not modified and operate at the same speed and data width as in the previous systems. A processor

board is upgraded with the Pentium and includes filtering logic according to the present invention. The Pentium includes eight byte-enable bits as compared to the four byte-enable bits used by the 386 and 486. Two new special cycles supported by Pentium are not supported by the previous host bus and would cause erroneous operation if allowed on the host bus. The filtering logic detects the two new cycles and prevents these cycles from being passed to the host bus.

 ${f 5,} {f 404,} {f 473}$  Apparatus and method for handling string op-

erations in a pipelined processor

Issued: April 4, 1995

Inventors: Papworth, David B., et al

Assignee: Intel Filed: March 1, 1994

Claims: 37

In a pipelined processor, when a string operation is received, the length of the string as specified by the programmer is stored in a register. Next, an instruction sequencer issues an instruction that computes the register value minus a predetermined number of iterations to be issued into the pipeline. Following the instruction, the predetermined number of iterations is issued to the pipeline. When the instruction returns with the calculated number, the instruction sequencer then knows exactly how many iterations should be executed. Any extra iterations that were issued initially are canceled by the execution unit, and additional iterations are issued as necessary.

**5,404,422** Speech recognition system with neural net-

work

Issued: April 4, 1995

Inventors: Sakamoto, Kenji, et al Assignee: Sharp Kabushiki Kaisha

Filed: February 26, 1993

Claims: 14

A voice-recognition apparatus capable of recognizing any word utterance by using a neural network. The apparatus includes a unit for inputting an utterance and for outputting a value corresponding to a similarity between the input and words to be recognized as determined by a neural network.

## **Other Issued Patents**

**5,408,639** External memory-access control for a processing system

**5,406,504** Multiprocessor cache examiner and coherency checker

**5,404,478** *Method of managing a virtual storage for a multiprocessor system* ◆