Most Significant Bits

Pentium Surges to 133 MHz

The latest delivery from the Pentium-of-the-month club is a 133-MHz version, the first product from Intel's 0.35-micron P54CS design *(see **090402.PDF**)*. The company continues to ramp production of its newest manufacturing process, which should yield 150-MHz parts by this fall. The 133-MHz Pentium is priced at $935 in 1,000-unit quantities, a 27% premium over the 120-MHz Pentium for an 11% increase in clock speed.

In a system with 1M of fast L2 cache, the new chip is rated at 155 SPECint92 and 116 SPECfp92. This integer performance is better than that of any shipping system except Digital's fastest Alpha workstations. Several recently announced RISC products will probably reach the market at about the same time as 133-MHz Pentium systems, keeping RISC performance at least slightly ahead of Intel's. In a standard PC motherboard, the 133-MHz chip delivers about 130 SPECint92.

The new chip supports Intel's continued effort to aggressively increase Pentium performance. More important, the presence of faster chips pushes devices such as the 100-MHz Pentium squarely into the PC mainstream. By getting to 0.35-micron technology ahead of the rest of the industry, Intel is making it more difficult for its competitors to compete.

AMD Ships Enhanced 486s

Giving its 486 line a significant boost, AMD has announced a new line of chips led by a clock-tripled 120-MHz 486DX4. Like AMD's earlier DX4, these chips have only half the cache of Intel's DX4, but a new write-back mode reduces accesses to the system bus. Also new is an Intel-compatible system-management mode (SMM) and STPCLK signal, making the chip fully pin-compatible with the Intel part (with additional write-back signals).

AMD's previous SMM implementation used Intel's in-circuit emulator (ICE) microcode, and a court ruling last fall forced AMD to take these parts off the market *(see **0815MSB.PDF**)*. The new chips use clean-room microcode that provides full Intel compatibility without using Intel's ICE microcode. These chips enable AMD to enter the notebook 486 market for the first time. The company is offering 75- and 100-MHz chips in a 208-pin SQFP for portable applications. AMD says that its 3.3-V 486DX4-100 consumes 1 W less than Intel's device.

For entry-level desktops, AMD pitches its 120-MHz 486 as a superior alternative to Pentium-75 processors. According to AMD's benchmarks, its DX4-120 is 13% faster than a Pentium-75 on Winstone 95. At about $165 in 1,000-piece quantities (official pricing has not yet been announced), AMD's part is priced more than $100 below the Pentium-75. In addition, 486 chip sets and motherboards are less expensive than those for Pentium, producing a total system cost savings of more than $200 while delivering equivalent performance—as long as floating-point performance isn't important.

The new chips use AMD's 0.5-micron process. Samples are available now, with production planned for the third quarter. Sources indicate that a 133-MHz version will follow late this year using a 0.35-micron design. AMD expects to ship more than 7 million 486 chips in the second half of this year, easily exceeding its goal of 10 million units for the year and accounting for more than 50% of all 486 shipments in the fourth quarter.

TI Samples 80-MHz 486DX2 at $1/MHz

Continuing to bottom-feed on the 486 market, Texas Instruments has introduced its first 486DX2 just as AMD is upscaling to 120-MHz devices. Like other TI 486s, the new part is based on Cyrix's original 486 core, which delivers slightly less performance at a given clock speed than AMD's or Intel's 486s. To gain entry into this market, TI is offering an aggressive price of just $1 per MHz: $66 for the 66-MHz DX2 and $80 for the 80-MHz version, both in quantities of 1,000.

TI builds its DX2 in its 0.5-micron EPIC-3 process *(see **080504.PDF**)*, although the Cyrix design uses only two metal layers. The die measures 80 mm^2, resulting in an estimated manufacturing cost of just $22. This cost gives TI a reasonable margin even at $1/MHz. The chip uses a 3.45-V supply and consumes 2.8 W (typical) at 80 MHz, about the same as a 75-MHz DX4 from Intel.

The Cyrix design uses a write-back cache, which reduces the number of system-bus accesses. Both Intel and AMD have recently added this feature to their own 486 chips, but many system makers are still using the older write-through parts. For these vendors, the TI part can offer a small performance boost, particularly for systems without an L2 cache.

Later this year, the company expects to announce a 486DX4 that includes clock tripling but not Intel's expanded cache. TI is also working on its own Pentium-class core, but products based on this core are much further in the future.

In the meantime, the company sees extensive interest in the 486 among home users in the U.S., from developers of embedded systems, and in emerging countries around the world. Intel is turning its back on the 486, encouraging PC users to switch to Pentium, while AMD and Cyrix are focusing on higher-speed 486 devices. As these vendors move up, TI hopes to scarf the leftovers in the DX2 market. With its expertise in low-cost manufacturing, TI is an excellent candidate to supply the low end of the 486 market after other vendors lose interest in it.

HP Rolls Out 120-MHz PA-7200 Systems

On the heels of its 100-MHz servers, HP has raised the speed of its PA-7200 and put it into a dual-processor workstation. The new J-series desktops deliver 169 SPECint92 and 269 SPECfp92 with a single processor. Entry pricing for the 120-MHz J210 is $41,770 for the uniprocessor and $54,770 for two processors. The systems are due to begin shipments in 3Q95, but HP does not expect volume shipments until late this year.

These systems set a new mark for PA-RISC performance and keep HP ahead of Sun's 125-MHz HyperSparc systems *(see **0906MSB.PDF**)*. Digital's Alpha workstations, however, deliver far better performance, and IBM's new 604-based workstations *(see **090803.PDF**)* offer equivalent integer performance for far less money. HP is waiting for the PA-8000 to restore the competitiveness of its product line, but that processor won't be available until 1Q96.

R4400 Reaches New Performance Level

NEC has announced sampling of a 250-MHz R4400. The company achieved this speed using a 0.35-micron process, which also shrinks the die to 108 mm^2. The company estimates that the new chip will achieve 175 SPECint92 and 178 SPECfp92. Production shipments are slated for the third quarter. NEC did not announce volume pricing; samples are available for $2,000.

The new version must satisfy high-end MIPS users until the R10000 is ready early next year. It keeps high-end MIPS performance competitive with most other RISC architectures, at least until UltraSparc and the PowerPC 620 become available late this year. Interestingly, the new R4400 has only 13% better integer performance than the 133-MHz Pentium and requires a 20% larger die in a similar 0.35-micron process, gaining no advantage from its streamlined RISC architecture.

Cypress Enters Pentium Chip-Set Market

Cypress's first Pentium chip set uses an innovative integrated cache to reduce cost while increasing performance. The HyperCache chip set consists of three chips: a PCI and memory interface, a data-path chip with integrated 128K cache, and a system I/O device. The chip set supports Pentium-class CPUs from Intel, AMD, and Cyrix *(see **090804.PDF**)* at bus speeds of up to 66 MHz.

Integrating a complete 128K cache and tags into a single package eliminates the cost of several packages from a typical discrete cache. Furthermore, timing is greatly improved, as critical signals are no longer driven from chip to chip. HyperCache uses a synchronous core to deliver 3-1-1-1 burst timing, yet the entire chip set costs little more than a discrete synchronous cache of the same size. System performance is further improved by the cache's two-way set-associative design; discrete caches are typically direct mapped due to pin-count limitations. Cypress claims that these features make its 128K cache comparable to a 256K asynchronous design.

The chip set includes a PCI-to-ISA bridge, EIDE support with bus mastering, DMA/interrupt control, a real-time clock, keyboard and mouse control, and power management, giving it a greater level of integration than Intel's popular Triton chip set. At $48 for the three-chip set, HyperCache carries about the same price as the cacheless Triton. The Cypress cache can be expanded in 128K increments at $14 each.

Cypress entered the chip-set arena by purchasing Contaq Microsystems, a 10-person design firm. Cypress itself is a leading supplier of cache chips for Pentium PCs, and this customer base should give its new product a quick entry into the high-volume chip-set market.

Somerset Seeks New Head

Seeking to streamline the decision-making process, IBM and Motorola have decided to reorganize their Somerset Design Center, the source of most PowerPC processor designs to date. Since its inception, the center has been managed jointly by IBM and Motorola personnel. This awkward structure has slowed progress in some areas and caused enough dissatisfaction that engineers have been leaving for greener pastures.

Given the lackluster results of the 604 and 620 *(see **0908ED.PDF**)*, a change is in order. The companies have now assigned a single leader for each project, replacing the old co-manager structure. They are also seeking a single manager to oversee all of Somerset, although it may take months to locate the right person. The partners hope that these changes will spur progress on the next generation of PowerPC designs. ♦

New Analyst Yong Yao

Yong Yao has joined MicroDesign Resources as our senior analyst for PC technologies. His latest work appears on the cover of this issue, and he will continue to write articles for *Microprocessor Report* covering chip sets, graphics, and other aspects of system design.

Yong comes to us from Vitesse, where he was the director of product planning as well as the designer of the multiprocessor V-Bus *(see **080701.PDF**)*. His experience also includes designing system-logic chip sets, graphics chips, and network interfaces as well as research at UC Berkeley. Yong has a PhD in electrical engineering from Shanghai Jiao-tong University.

His primary role with MDR will be to direct our Technology Roadmap service, which provides detailed information on PC system design trends, including analyses of current products and projections of future configurations and technology trends. For more information about this service, contact Yong at our editorial office.

