Patent Watch

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently:

5,421,020
Counter register implementation for speculative execution of branch-on-count instructions
Issued: May 30, 1995
Inventors: David S. Levitan, et al
Assignee: IBM
Filed: January 8, 1993
Claims: 6
A data-processing system for speculatively executing instructions includes a memory for storing instructions at addresses that can be generated by a branch unit in a processor. The processor also has a count register for storing an update value, a dispatch version value, and a completion version value. A fetcher connected to the branch unit fetches instructions from memory based upon addresses calculated by the branch unit. The system further includes means responsive to dispatch of a conditional branch instruction for examining the dispatch version value to determine if a branch should be taken and then decrementing the dispatch version value. Means responsive to completion of the branch provides for decrementing contents of a completion version register.

5,420,992
Backward-compatible computer architecture with extended word size and address space
Issued: May 30, 1995
Inventors: Earl A. Killian, et al
Assignee: Silicon Graphics
Filed: April 5, 1994
Claims: 17
A technique for extending the data word size and the virtual address space of a pre-existing architecture so that hardware for the extended architecture also supports the pre-existing architecture. Extension of the data word size from M bits to N bits entails widening the machine registers and data paths from M bits to N bits and sign-extending entities of M or fewer bits to N bits when they are loaded into registers. Some of the M-bit instructions, when operating on N-bit sign-extended versions of M-bit entities, can produce incorrect results. For these instructions, compatibility requires that separate N-bit instructions corresponding to these M-bit instructions are needed. The support for up to an N-bit virtual address space is provided in part by widening the virtual address data paths. The extended architecture supports the M-bit architecture's addressing by storing M-bit addresses as N-bit entities in sign-extended form and requiring that the results of address computations on these entities be in sign-extended form.

5,420,990
Mechanism for enforcing the correct order of instruction execution
Issued: May 30, 1995
Inventors: Francis X. McKeen, et al
Assignee: Digital
Filed: June 17, 1993
Claims: 3
An apparatus for ensuring that selected instructions are executed in a correct order, comprising a first content-addressable memory for storing load addresses of data read from the memory by the selected instructions. A first content-addressable memory compares the store addresses with the load addresses of data to be written to the memory. The first content-addressable memory generates a first signal if one of the load addresses is identical to a subsequently compared store address. The apparatus further includes a second content-addressable memory for storing and comparing states of the data read and written by the selected instructions. The second content-addressable memory generates a second signal if one of the stored states is identical to one of said compared states. The stored states include a program counter to repeat the execution of the selected instructions upon detecting the first and second signals.

5,420,989
Coprocessor interface supporting I/O or memory mapped communications
Issued: May 30, 1995
Inventors: Robert D. Maher, III, et al
Assignee: Cyrix Corporation
Filed: June 12, 1991
Claims: 8
A coprocessor comprises a bus controller, which further comprises a primary bus controller and a secondary bus controller that drive a floating-point processor core. The primary bus controller comprises a memory-mapped bus interface for processing memory-mapped format instructions and an I/O bus interface for processing conventional I/O format instructions. The primary bus controller remains essentially transparent for execution of I/O format instructions and translates memory-mapped format instructions into sequential bus cycles compatible to an I/O bus interface for processing conventional I/O format instructions, and for execution by the floating-point processor core. ♦

