Glossary

This glossary briefly describes acronyms and abbreviations that are frequently used in Microprocessor Report and will be included here on an occasional basis. Abbreviations not listed here will be defined when used.

ABI—Application Binary Interface; a software definition that describes the binary instruction encodings for a particular processor along with API compliance.

ADC—Analog-to-Digital (A/D) Converter; a circuit that generates a binary (numeric) description of an analog voltage level.

ALU—Arithmetic Logic Unit; a circuit that performs math calculations and/or logical operations.

API—Application Programming Interface; a software definition that describes operating system calls for applications software that may be used across a range of processors (see ABI).

ASIC—Application-Specific Integrated Circuit; a chip designed for a particular customer or system, typically from standard cells and/or gate arrays. May ultimately be sold as a standard part.

BAPCo—Business Applications Performance Corporation; a set of benchmarks for PC applications focusing on system performance *(see **061302.PDF**)*; results are reported as SYSmark92.

BiCMOS—Bipolar CMOS; an IC manufacturing process combining bipolar and CMOS circuits *(see **070703.PDF**)*.

BIOS—Basic I/O System; ROM-based software in a DOS system that interfaces directly to the hardware to perform input/output and other low-level functions.

BitBLT—Bit Block-Transfer; a graphics operation that copies arbitrarily aligned data from one portion of memory to another *(see **061301.PDF**)*.

bps, kbps, Mbps—bits per second, thousands (1000s) of bits per second, millions (1,000,000s) of bits per second; units of measure for data-transfer rates.

COSE—Common Open Software Environment; a group of vendors that plans to establish a common Unix standard *(see **0707MSB.PDF**)*.

CISC—Complex Instruction Set Computing; refers to processors (e.g., the 680x0 and x86 families) with variable-length instructions that typically execute in multiple clock cycles.

CMOS—Complementary Metal-Oxide Semiconductor; a common IC manufacturing process for low-power, high-density chips *(see **070703.PDF**)*.

CPU—Central Processing Unit; a chip or circuit that interprets and executes program instructions.

DAC—Digital-to-Analog (D/A) Converter; a circuit that generates an analog voltage level from a binary (numeric) value.

DMA—Direct Memory Access; a method of moving data from memory to I/O without using the CPU.

DSP—Digital Signal Processor; a processor optimized for multiply-accumulate operations and high data rates for real-time applications.

EISA—Extended Industry Standard Architecture; a 32-bit version of the ISA bus (see MPR 10/88, p. 1).

ExCA—Exchangeable Card Architecture; a software standard for PCMCIA cards *(see **061604.PDF**)*.

FIFO—First In, First Out; a buffer that stores and forwards data items in the same order in which they are received.

FP—Floating Point; a type of math that handles very small and very large numbers, typically used for scientific calculations.

FPU—Floating-Point Unit; a chip or circuit that performs floating-point math calculations.

GUI—Graphical User Interface; software that interacts with the user by means of menus, windows, and icons (e.g., Windows, Macintosh).

IC—Integrated Circuit; a chip.

ISA—Industry Standard Architecture; a 16-bit expansion bus commonly used in PCs; also known as the PC/AT bus or AT bus after the IBM system that first used it.

ISV—Independent Software Vendor; a company that develops and markets application software.

JPEG—Joint Photographic Experts Group; an international standard for still-image compression that achieves a high rate of compression by allowing limited degradation from the original image.

MCA—Micro Channel Architecture; a 32-bit expansion bus developed by IBM for its personal computers (see MPR 11/87, p. 1).

MESI, MOESI—cache coherency algorithms used in multiprocessor systems (see MPR 6/20/90, p. 12); the letters represent the possible states: modified, owned, exclusive, shared, and invalid.

MIPS—Millions of Instructions Per Second; a misleading indicator of processor speed unless it is attached to some benchmark (e.g., Dhrystone 2.1).

MMU—Memory-Management Unit; a chip or circuit that translates virtual memory addresses to physical addresses and may implement memory protection.

MP—Multiprocessor; a system with more than one processor, typically used to refer to systems with more than one central processor.

MPEG—Motion Picture Experts Group; a set of international standards for video and audio compression that allows limited degradation to achieve high compression rates *(see **060803.PDF**)*.

OEM—Original Equipment Manufacturer; a vendor that combines hardware and/or software from others, adds its own products, and sells the resulting combination to end users.

OS—Operating System; software that handles basic system chores such as memory management, process scheduling, and input/output; accessed by application software through a defined API.

OSF—Open Software Foundation; a consortium that was founded by HP, IBM, and DEC to create a Unix alternative to AT&T's System V.

OTP—One-Time Programmable; see "PROM."

PC—Personal Computer; an IBM-compatible (or similar) desktop or portable system; includes products such as Apple Macintosh or Alpha-based PCs.

PC board—Printed-Circuit Board (PCB); a system board or add-in card that contains a number of chips, sockets, discrete components, and connectors.

PCI—Peripheral Component Interconnect; a bus that connects high-speed peripherals to the processor *(see **060902.PDF**)*.

PCMCIA—PC Memory Card Industry Association; an electrical and physical standard for add-in cards primarily intended for portable systems *(see **061604.PDF**)*.

PDA—Personal Digital Assistant; a handheld computer that can be programmed with software from multiple vendors (e.g., Apple Newton).

PGA—Pin-Grid Array; an IC package that has multiple rows of pins on the bottom *(see **071004.PDF**)*.

PLL—Phase-Locked Loop; a circuit that synchronizes two clock signals, often used in microprocessors to generate a 2× (or other integer multiple) frequency.

PQFP—Plastic Quad Flat Pack; an IC package that has a single row of pins around all four sides *(see **071004.PDF**)*.

RAM—Random Access Memory; information can be written to this chip and quickly retrieved from any internal location. **DRAM** must be repeatedly "refreshed" to maintain its contents. **SRAM** does not need to be refreshed. **VRAM** is like DRAM but has a second, serial port for reading its contents.

RAMDAC—A graphics chip that usually has three 8-bit DACs and a small RAM to store color translations. The DACs generate red, green, and blue outputs for an analog monitor. The RAM translates a 4- or 8-bit color specifier into a 24-bit output.

RISC—Reduced Instruction Set Computer (see MPR 8/7/91, p. 16); refers to processors with limited address modes and short (≤32 bits), fixed-length instructions that typically execute in a single cycle (e.g., MIPS, SPARC).

ROM—Read-Only Memory; a chip that stores information but cannot be written to. **PROM** can be programmed once only. **EPROM** can be erased by exposure to ultraviolet light and then reprogrammed; **EEPROM** can be electronically erased but takes much longer to program than to read.

SIMM—Single In-line Memory Module; a standard add-in board for memory expansion.

SMM—System-Management Mode; a special mode on x86 processors that is more privileged than protected mode; often used for power management.

SPEC—System Performance Evaluation Cooperative; a set of benchmarks for workstation applications *(see **061204.PDF**)*; integer performance is reported as **SPECint95** and FP performance as **SPECfp95**.

TAB—Tape Automated Bonding. A low-cost IC packaging method that attaches a die directly to a PC board using a thin film with conductive leads *(see **071304.PDF**)*.

TLB—Translation Lookaside Buffer; a local cache memory for virtual-to-physical address translations; usually part of the MMU.

VL-Bus—VESA Local Bus; a 486-like bus, defined by the Video Electronics Standards Association, that connects graphics chips and other high-speed peripherals to the processor *(see **060902.PDF**)*. ♦

