THE EDITOR'S VIEW

Emulation Could Unburden CPU Designers

Native Instruction Set May Become Unimportant by End of Decade

Digital's recently unveiled x86 emulation technology, dubbed FX!32 *(see* ***0916MSB.PDF****)*, is a taste of things to come. With other major microprocessor vendors also pursuing high-performance emulation, it is only a matter of time before this technology becomes effective and widespread. The main goal of emulation is to free end users to switch from one platform to another. It could also end up freeing CPU designers from the burden of instruction-set compatibility.

Nearly all of today's microprocessors are designed to be compatible with existing instruction sets, taking advantage of the installed base of software for that architecture. System vendors fear breaking this model, as many have lost customers during rocky transitions from one instruction set to another. As a result, most current processors execute instruction sets that were created a decade ago or more.

The problem with this model is that there is a tight relationship between instruction-set design and the technology tradeoffs of the moment. CISC instructions were designed to be interpreted one byte at a time and executed serially on a simple microengine, hence the use of variable-length encodings and variable execution times. The lack of caches at the time is reflected in allowances for self-modifying code.

RISC became a superior alternative when buses grew wide enough to fetch a complete 32-bit instruction at once. RISC instructions were designed for efficient pipelining, but executing them in a single cycle required a larger transistor count than a simple microengine. Fortunately, the IC processes of the mid-1980s fit a complete RISC processor on a single chip. The greater transistor count also enabled an increase in the number of registers, supporting the emerging use of compilers.

These examples show how hardware changes that took roughly five years had a huge effect on instruction-set design. With transistor counts tripling every four years, the optimal instruction-set design continues to change rapidly, yet compatibility forces vendors to use older architectures that are mismatched to current manufacturing technology, reducing their performance.

In contrast, vendors that introduce new high-end instruction sets frequently gain the performance lead. For example, the MIPS R2000, Intel's i860, Digital's Alpha, and IBM's POWER all debuted at number one on the performance charts.

Some would argue that Pentium Pro's stealing the integer performance lead from Alpha shows instruction sets are irrelevant to performance. In fact, however, Intel's performance lead is mainly due to an advantage in manufacturing technology. In the same IC process, RISC chips can (and do) deliver better performance. The gap would be larger, except that RISC architectures are nearly as outdated as the x86 instruction set.

Neither RISC nor CISC is well suited for the complex superscalar processors being designed today. The optimal instruction set for modern processors would be designed to execute large numbers of operations in parallel by allowing the compiler to provide hints for instruction grouping and for branch prediction, for example. A larger register set would also be useful.

Intel and HP are the first major vendors to realize that both CISC and RISC are suboptimal, and they are jointly developing a new instruction set intended for processors with 10 million transistors or more. This will be the first major high-end instruction set since Alpha debuted in 1992. Like Alpha, the Intel/HP chip should outperform all other microprocessors when it appears.

With the appropriate emulator/translator, any vendor can now move to a new instruction set carefully optimized for the IC technology of the day. As long as low-level software (operating systems and drivers) and key performance-sensitive applications are available in the new native format, the gains for most users will outweigh the minor performance loss on legacy software.

Apple has demonstrated that such a transition can be made with minimal pain to the end user. Apple's emulator matches the performance of its older systems only because those systems are relatively slow. With the improved performance offered by FX!32-like translation, other vendors could use a similar strategy.

By the end of the decade, instead of coalescing around a couple of standard instruction sets, processor vendors could use binary translation to enable a new round of innovation. Removing the weight of compatibility would level the playing field, giving other vendors a good shot at matching or beating the Intel/HP chip. As an added benefit, any processor could run applications designed for any other chip with a significant software base. May the best CPU designers win! ♦

Will binary translation enable new instruction sets, or will x86 continue to dominate the microprocessor industry? Send your opinion to editor@mdr.zd.com.

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