MOST SIGNIFICANT BITS

Intel Rolls Out Pentiums at 150, 166 MHz

Extending its main product line, Intel announced immediate availability of Pentium processors at speeds of 150 and 166 MHz. The new speed grades, carrying 1,000-piece list prices of $547 and $749, fill the gap between the $520 Pentium-133 and the least-expensive Pentium Pro, which lists for $974. Although the price of the Pentium-150 nearly coincides with that of the 133-MHz version, we expect the price cuts scheduled for February 1 will create a bigger gap.

The announcement was hardly a surprise; a few PC vendors jumped the gun and began advertising 150-MHz systems in December. Sources indicate that the 150-MHz part was initially planned for a 4Q95 release but was delayed to avoid confusing holiday buyers. Certainly, there was no technical reason to delay the introduction; the faster speeds come from the 0.35-micron P54CS design, which has been shipping since last summer; we believe it has been yielding reliably at 150 MHz for months.

The new chips reassert Intel's performance lead over its x86 competitors. Both Cyrix and NexGen are shipping chips that they claim match the integer performance of a Pentium-133, although falling behind in the FP area; Intel now takes a clear step ahead until these competitors can also improve their clock speeds. At 4.8 SPECint95 and 2.7 SPECfp95 (base), the 166-MHz Pentium nearly matches the latest integer numbers for the PowerPC 604-133 *(see* **1001CW.PDF***)*, but Pentium's FP score is still well behind.

The new chips use 2.5× clock multipliers. The Pentium-166 uses a 66-MHz bus and thus can upgrade 100- and 133-MHz motherboards. The Pentium-150 requires a 60-MHz bus. Because of the lower bus speed, the 150-MHz part is only 3% faster than a Pentium-133 on SPECint95 and is actually slower on SPECfp95. With a 256K cache, the Pentium-150 will be slower on many PC applications as well, but unenlightened end users will probably snap it up.

The Pentium line is not yet out of steam; we expect Intel will squeeze a 180- or 200-MHz part out of the current P54CS design, and the P55C Pentium should easily hit those speeds. At such high speeds, the 8K caches of the P54CS become a bottleneck, limiting the performance gain, but as with the Pentium-150, this will not affect the decision of most system buyers. The P55C will enlarge the caches to 16K each, improving performance at higher speeds.

Philips Produces Single-Chip PDA Processor

Stepping squarely into the 32-bit embedded microprocessor arena, Philips has begun sampling an integrated MIPS chip for PDAs and other handheld applications. The PR30100, also called the OneChip PDA, offers an impressive level of on-chip I/O, integrating an R3000 core, LCD controller, touch-screen support, audio DAC, IrDA (infrared) interface, real-time clock, and UART in one package. Only a touch-sensitive LCD screen, batteries, and memory are required to create a basic PDA. Samples of the device are now being evaluated at Philips' own consumer-electronics division and by unannounced third-party developers.

Performance is not the 30100's strong point. To reduce power, the chip operates at a relatively pokey 18.432 MHz. (The odd frequency is generated by an on-chip PLL from a standard low-cost watch crystal.) Even with its dual 1K caches and single-cycle execution, the chip is among the slower new processors for handheld devices. Its on-chip circuitry for monitoring a touch screen makes it suitable for handheld units without keyboards, but its performance makes it better suited to applications where the user taps icons on the screen rather than for handwriting recognition. General Magic's rumored port of its Magic Cap operating system to the MIPS instruction set would seem to confirm those suspicions.

The new chip is the first MIPS product to come out of Philips since the company's acquisition of HDL Systems *(see* **0814MSB.PDF***)*. The 30100 is based on the MR300 core, a basic R3000 CPU designed by HDL. Philips is currently modifying the basic MR300 core, adding branch-likely instructions and other R4000-inspired extensions. This parallels a similar strategy at virtually every other MIPS licensee, including Toshiba, IDT, LSI Logic, and NEC, which have all extended the MIPS II instruction set in one way or another. Philips expects to announce the first processors based on the newer core in March. The company is also working to integrate the MIPS integer core with its own DSP unit for products in 1997.

The 30100 is a static 3.3-V device housed in a 160-lead PQFP. The chip is currently sampling, with production scheduled for March. Priced at less than $20 in 100,000-unit quantities, the 30100 offers impressive integration for the money. At less than 20 MHz, however, the chip's performance will not break any records. For performance-minded designers, Philips is developing additional cores with extended instruction sets and higher clock rates.

P7 Becomes Merced

Intel let slip a few more facts about the chip formerly known as P7, the first being that the project (like all Intel projects after the P55C) now has a name—Merced—instead of a number. Merced will be the first chip to implement the 64-bit instruction set, which Intel calls IA-64, created by the Intel/HP partnership. The company would not discuss the exact status of the project, but it is early in the design stage with shipments "a few years" away; we still project first shipments in late 1998.

Interestingly, Merced is being designed entirely by Intel engineers; HP helped define the instruction set and software interfaces. We believe that HP is separately developing its

own IA-64 processors. Intel said that all IA-64 chips will be built and sold by Intel, regardless of which company designs them; this ensures a level playing field between HP and Intel's other customers.

Intel continues to develop higher-performance products in its 32-bit x86 line; in addition to a 0.25-micron shrink of Pentium Pro that pushes clock speeds beyond 300 MHz, we expect to see in 1997 an improved version of the "dynamic execution" core that delivers even greater performance. For at least a few years, Intel will introduce chips from both the 32- and 64-bit families, but the company expects to eventually transition completely to the 64-bit instruction set, much like the transition from 16 to 32 bits implemented between the 286 and 386 generations. It remains unclear how long the 64-bit transition will last.

Intel affirmed that Merced will be fully compatible with x86 binaries at the hardware level, that is, no extra software will be required to emulate or translate these binaries. The company would not discuss the level of performance expected in x86 mode but admitted it would be less than in native IA-64 mode. The situation could be similar to the differences in 16- and 32-bit performance on Pentium Pro. Merced will also execute PA-RISC code, but we believe some software assistance will be required in this case.

AMD Gains Access to Intel Patents, MMX

Completing the settlement of their long-standing legal dispute *(see* **0901MSB.PDF***)*, Intel and AMD have agreed on a five-year patent cross-licensing agreement. This agreement is essential for AMD to continue designing and marketing x86-compatible processors without legal attacks from Intel. From Intel's standpoint, the agreement provides access to AMD's own patent portfolio and includes royalty payments from AMD; the specific terms were not disclosed, but AMD considers the royalties to be "not burdensome."

The agreement also gives AMD access to "certain copyrights" but not any microcode copyrights. AMD says, with this agreement in hand, it has all the copyrights and patent rights necessary to implement Intel's forthcoming multimedia extensions, known as MMX, in its future processors, although there is no specific transfer of this technology. NexGen had already announced plans to include MMX-like extensions in its 686 *(see* **091401.PDF***)*, now the AMD K6; the K6 extensions will be made MMX-compatible, although possibly not by the first release.

AMD's support for MMX leaves Cyrix in an awkward position. That company has already developed its own multimedia extensions but is unlikely to garner much support for them if the two biggest x86 vendors back MMX. Cyrix has access to MMX patents, but not copyrights, through its foundries; AMD expects these copyrights to be a barrier, but since they mainly cover instruction mnemonics, we expect Cyrix and others will be able to work around them. Unfortunately, these vendors will need extra time to convert their efforts to be MMX-compatible. We expect all the major x86 vendors to adopt MMX, but Intel and AMD are likely to have a 6–12-month lead over their competitors.

One thing the Intel/AMD agreement omits is access to the Pentium Pro bus. AMD is permitted to implement variations on that bus, but its processors cannot be exactly pin- or protocol-compatible with Intel's. Third-party chip sets could support both types of processors in this scenario, but Intel's own chip sets would, of course, not support AMD's processors. Thus, the agreement ensures a common software base for x86 processors but prevents AMD devices (after K6) from simply "stealing sockets" from Intel.

Intel OverSPECs Parts

A red-faced Intel spokesman admitted that the company's reported SPECint92 scores for the past several months have been inflated by roughly 10%. The problem was nominally caused by a bug in Intel's beta compiler used for generating the code for the 023.eqntott benchmark, eliminating certain required operations. Intel did not immediately notice the problem because the erroneous code still generated the correct answer. The bug more than doubled the eqntott score and, due to the magic of the geometric mean, increased the overall SPECint92 score by about 10%.

Because eqntott is not included in the SPECint95 suite, the error does not impact that metric. Therefore, it does not affect most recent performance comparisons in *Microprocessor Report*, since we have moved to the newer SPEC95 suite and no longer report SPEC92 data. Because the bug is in an unreleased version of the compiler, it does not affect any production code.

The problem does expose the seamy underside of the SPECsmanship played by Intel and other major vendors. To increase the eqntott score by a factor of two, Intel modified its compiler to look for certain unique sequences that occur in that program and replace them with hand-optimized assembly code. This benchmark-specific optimization is legal under SPEC rules (including SPEC95) and is widely practiced. Unfortunately for Intel, its optimized code could have generated incorrect results with data other than the prescribed values for the SPEC test.

This mistake came to light only after Motorola began investigating Intel's suspiciously high eqntott score. Intel cooperated by supplying its binaries, and Motorola found the offending routine; Intel immediately made a public disclosure and apology. It appears the error was inadvertent, but as the episode shows, vendors that push benchmarking rules to the limit will occasionally go over the edge.

NEC Tapped to Build MicroSparc-3 for Sun

Sun's SPARC Technology Business (STB) has unofficially settled on NEC as the foundry for its next-generation low-end processor, although a definitive agreement has not yet been signed. The new chip, called MicroSparc-3 in previous Sun roadmaps, is a 64-bit SPARC V9 implementation with integrated logic. Although the on-chip system logic is likely

to be similar to the MicroSparc-2 design, the V9 core will be derived from UltraSparc but modified to reduce cost.

Aimed for the low-end workstation, server, and embedded markets, the new chip is expected to reach production in 1H97, a bit later than previously planned *(see* **081301.PDF***)*. Sources indicate that NEC, acting only as a foundry for STB, will have no design or marketing rights to the new device. TI will continue to fabricate high-end UltraSparc processors for Sun workstations.

SGS Offers 486 Core

SGS-Thomson has made its speedy 486DX4 processor core available as part of the company's ASIC library, merging the high-speed, static core with a number of flexible peripheral modules. The announcement marks the first time that an x86 core has been made available for custom designs.

SGS's new core includes an FPU and a unified 8K cache that operates in either write-through or write-back mode. The core operates over a voltage range of 2.2 to 3.6 volts and is completely static, allowing ASICs to power down when not in use. For PC-like applications, SGS's macrocell library includes PCI, IDE, ISA, and MIDI interfaces, DRAM controllers, and memory blocks—some developed by SGS, some licensed from other companies.

SGS's 0.35-micron four-layer-metal process reduces the 486 core size to just 51 mm^2. The advanced process also increases the clock speed to 120 MHz, making it one of the fastest 486 chips available and far faster than any other embeddable x86 core. While both Vadem and AMD market devices with embedded x86 cores (the VG3x0 and 386SC, respectively), both are in the 386 performance class. In addition, neither company has the broad ASIC experience or peripheral library of SGS-Thomson, making the European firm attractive for designers who want something beyond a simple PC-on-a-chip.

UMC Exits 486 Business

United Microelectronics Corp. (UMC) of Taiwan has agreed to pull out of the 486 microprocessor business as part of a settlement with Intel. Intel had sued UMC and its distributors in four countries *(see* **0909MSB.PDF***)*. In response, UMC had filed challenges to several Intel patents in Europe and Asia *(see* **0913MSB.PDF***)*. The two companies agreed to drop all pending actions. UMC will pay Intel an undisclosed sum, said to be less than $5 million, to cover legal expenses, and will cease sales of 486 processors.

With the rapid decline of the 486 market, it presumably was not worthwhile for UMC to fight Intel in court. UMC was also handicapped by its chips' slow clock rates and its decision not to sell chips in the United States. Intel was motivated to settle to avoid the possibility that UMC would succeed in overturning some of its patents, opening the door to other competitors. The fate of UMC's Pentium-class processor plans remains unknown; the company did not get any Intel patent rights as part of the settlement.

PowerPC Pumps Up Volume in 1995

According to new figures from analyst Andrew Allison, HP's PA-RISC architecture retained its title as the RISC system revenue champion in 1995, but in overall RISC volume, Hitachi's SH family took the lead, propelled by its monster Sega win. By both measures, PowerPC posted impressive increases, and it should surpass PA-RISC in the revenue category next year.

	1995		1994		Annual Growth
	Share	Revenue	Share	Revenue	
1) PA-RISC	30%	$12.5 B	33%	$9.6 B	+30%
2) PowerPC*	28%	$11.8 B	18%	$5.4 B	+119%
3) SPARC	17%	$6.9 B	20%	$5.8 B	+19%
4) MIPS	16%	$6.8 B	18%	$5.2 B	+31%
5) Alpha	6%	$2.5 B	5%	$1.5 B	+67%
6) Other**	3%	$1.2 B	6%	$1.8 B	–33%
	100%	**$41.7 B**	**100%**	**$29.3 B**	**+42%**

*includes POWER **includes Clipper, 88K, and others

The system revenue figures reflect the total system price of all general-purpose (nonembedded) RISC systems sold. With Apple's RISC conversion in full swing, PowerPC gained nearly 10 points of share, coming within 2 points of PA-RISC. Alpha, aided by Digital's own conversion, was the only other RISC to gain share but remains mired in last place; SPARC was the biggest share loser. Overall, RISC system revenue surged an impressive 42%. Excluding PowerPC, revenue improved by 25%, similar to growth in the PC market but, of course, from a much lower base.

	1995		1994		Annual Growth
	Share	Units	Share	Units	
1) SH	41%	12.0 M	18%	2.8 M	+329%
2) i960	20%	5.9 M	34%	5.2 M	+13%
3) PowerPC*	11%	3.3 M	12%	1.8 M	+83%
4) MIPS	11%	3.1 M	11%	1.7 M	+86%
5) ARM	7%	2.1 M	8%	1.2 M	+75%
6) 29000	6%	1.8 M	9%	1.4 M	+33%
7) SPARC	2%	0.7 M	4%	0.6 M	+21%
8) Other**	2%	0.5 M	4%	0.6 M	–11%
	100%	**29.4 M**	**100%**	**15.2 M**	**+94%**

*includes POWER **includes Transputer, Alpha, and others

Allison's figures, which do not include PA-RISC, put SH shipments at 12 million for 1995, nearly all from the Sega Saturn game player, each of which incorporates three SH processors. Intel's i960 falls to the number-two spot and continues to trail the market in growth. We expect PowerPC's surge will propel it past Intel's RISC chip in 1996 volume. MIPS and ARM are also hot, due to the success of both in the embedded market. With AMD's 29K in the graveyard and other RISCs stalling or fading, the market appears to be winnowing the choices. ♦

